CONTROL DATA®
CENTRAL COMPUTER

AA102-A

INSTALLATION AND
CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE AIDS
PARTS DATA

Volume 2

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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	5-219, 5-220.1, 5-221, 5-224, 5-225, 5-247, 5-270, 5-271, 5-277, 5-279, 5-287, 5-289, 5-295, 5-301,
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	5-306.3, 5-308.1, 5-335, 5-339, 5-347, 5-349, 5-353, 5-363, 5-365, 5-381, 5-389, 5-409,
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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

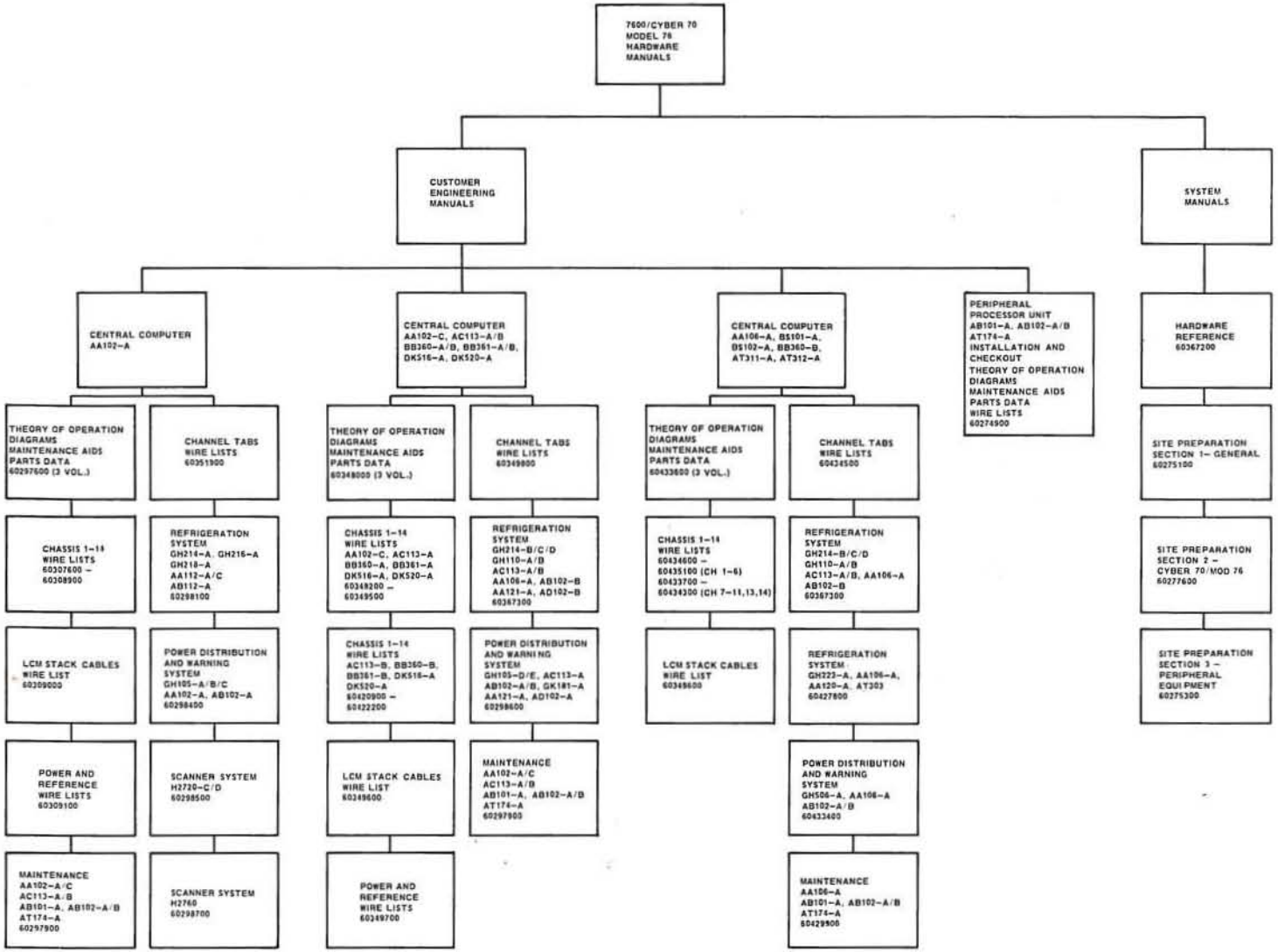
EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AA102-A	A01		Released
	A02	FCO24909	
	A03	FCO24512	
	A04	FCO25139	
	A05	FCO25648	
	A06	FCO26353	
	A07	FCO26669	
	A08	FCO27008	
	A09	FCO27240	
	A10	FCO28004	
	A11	FCO27678	
	A12	FCO27817	
	A13	FCO28306	
	A14	FCO28522	
	A15	FCO29030	
	A16	ECO27926	
	A17	FCO29125	
	A18	FCO29720	
	A19	FCO30674	
	A20	FCO29127	
	A21	FCO31865	
	A22	FCO31284	
	A23	FCO32459	
	A24	FCO30839	
	A25	FCO31505	
	A26	FCO33290	
	A27	FCO33261	
	A28	FCO33714	
	A29	FCO33798	
	A30	FCO34625	

PREFACE

This manual contains information pertaining to the AA102-A Central Computer. Comparable information on the AB101 Peripheral Processor Unit (including the Maintenance Control Unit) is contained in the PPU CE manual 60274900.

The System Publication Index on the next page graphically lists the related publications. Refer to the Literature Distribution Service Catalog for the latest revision of each of the related manuals.



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SECTION 5

PART 4

SMALL CORE MEMORY

The SCM is a 32-bank coincident current type memory with a capacity of 65,536 65-bit words (including five odd parity bits per word). Each bank is independent of the other 31 banks. Sequentially addressed words reside in sequential banks. This allows a maximum data transfer rate of one word each clock period. Each bank has a four clock period access time from arrival of the address to readout of the word. The total read/write cycle time for a bank is ten clock periods. Therefore, it is possible for a maximum of ten banks to be in operation at one time. This occurs during block copy instructions between SCM and LCM in which sequentially addressed words cannot cause SCM conflicts. In random addressing of SCM, an average of four banks in operation at one time is normal.

ADDRESS PATHS

There are four sources for addresses to SCM. These are IFA Register, BAK Register, Increment Unit, and I/O Multiplexer. The IFA and BAK Registers are each used for two functions. Therefore, six basic functions require an SCM reference. The SCM Access Control determines the priority when two or more of these functions request an SCM reference in the same clock period. Only one address may be accepted in a given clock period, and the choice is dictated by the following priority list:

1. Exchange sequence request (BAK Register)
2. Increment Unit request
3. Return jump exit request (IFA Register)
4. I/O Multiplexer request
5. Instruction fetch request (IFA Register)
6. LCM block copy request (BAK Register)

IFA REGISTER

The IFA circuit contains two operand selection networks, two operand holding registers, and an adder. The adder output is gated into the SAS under control of the Access Control. There are three possible outputs from the IFA adder. They are (RAS) + (P), IFA +1, or IFA +0.

BAK REGISTER

The BAK Register and its associated static networks form the mechanism for counting thru the 16 address values required in an exchange sequence. The initial exchange sequence address is XJA bits 0-15. The address value is incremented by one as each address is entered into the SAS. The incrementing is continued until all 16 addresses have been entered in the SAS. This process is controlled by the Access Control.

The BAK Register and its associated static networks also form the mechanism for counting thru all of the SCM addresses in an SCM to LCM or LCM to SCM block copy. The initial address is A0 + RAS Bits 0-15. The address value is incremented by one as each address is entered into the SAS. The incrementing is continued until all block copy addresses have been entered in the SAS. This process is controlled by the Access Control.

STORAGE ADDRESS STACK (SAS)

The SAS is a holding area for addresses arriving at the SCM. There are three 20-bit registers in the SAS which are referred to as Rank A, Rank B, and Rank C. These registers hold a 16-bit SCM address and a four-bit destination code. The Destination

Code Tag Bits are sent to the Destination Control where they are interpreted. Control signals are then generated to allow SCM data to enter the selected destination register at the proper time. If no SCM bank conflicts occur, an address enters SAS Rank A in any given clock period and leaves in the following clock period. SAS Ranks B and C are not involved even if a new address enters Rank A every clock period.

When an SCM bank conflict occurs, the address in Rank A is held until the conflict is resolved. If another address arrives at the SAS at this time, it will enter Rank B. When this occurs, no more addresses will be issued to the SAS until the backup condition has been resolved. There may be one address being processed in the Increment Unit at this time. If so, this address will enter Rank C. No new addresses will be accepted until all previously entered addresses have left the SAS. The addresses leave the SAS in the same order in which they entered.

STORAGE SEQUENCE CONTROL

Address Bits 0-4 are sent from the SAS to the Storage Sequence Control. These lower five address bits determine which of the 32 SCM Banks has been selected for a read/write cycle. The selected bank will receive a Go Bank signal if its previous read/write cycle has been completed. This is indicated when the selected bank generates a Free Bank signal.

BANK ADDRESS

Address Bits 5-15 are sent from the SAS to all SCM Banks. However, only the bank which has received a Go Bank signal will use the address bits.

PARITY ERROR ADDRESS REGISTER

Address Bits 0-15 leave the SAS and arrive at the Parity Error Address Register after a delay of six clock periods. This register is monitored by the MCU Scanner. SCM addresses are entered into this register every clock period if none of the Parity Error Bits 60-64 bits are set. When a parity error does occur, one or more of these bits will be set. This blocks entry of any subsequent addresses in the SCM Parity Error Address Register. Therefore, the SCM address at which the parity error occurred is held in the register.

WRITE DATA PATHS

STORAGE WORD STACK (SWS)

The SWS is a buffer area for 60-bit data words which are to be written into SCM. There are seven ranks (SWA-SWG) of 60-bit registers in this stack.

SWA is the first rank of the SWS. This register is normally cleared and entered with (Xi) during each clock period. This data is shifted through the seven ranks of SWS and written into SCM only when an increment instruction is issued which requires an SCM write reference. In all other cases the data is shifted through the ranks and discarded. This normal mode of operation is altered in the event of an SCM conflict or when an exchange sequence request is issued. An SCM conflict occurs when a bank cannot accept an address from the SAS because the previous read/write cycle for the selected bank has not been completed. In this case, the data is held in SWA until the conflict has been resolved. When an exchange sequence request is issued, the first eight 60-bit words of the exchange package are shifted through the SWS into SCM. The last eight words of the exchange package consist of X register data which is shifted through the SWS in the normal mode of operation.

SWB is the second rank of the SWS. This register is normally cleared and entered with (SWA) during each clock period. This normal mode of operation is altered in the event of an SCM conflict or when a return jump instruction is issued. In the event of an SCM conflict, the data is held in SWB until the conflict has been resolved. When a return jump instruction is issued, the RJX address is entered into bit positions 30-47 of SWB. The remaining bit positions of the 60-bit word become logical zeros except bit 56 which becomes logical one. This instruction word produces an unconditional jump to the RJX address.

SWC is the third rank of the SWS. This register is normally cleared and entered with (SWB) during each clock period. In the event of an SCM conflict, the data is held in SWC until the conflict has been resolved.

When a complete memory backup occurs, data held in SWC corresponds to SAS Rank A, data held in SWB corresponds to SAS Rank B, and data held in SWA corresponds to SAS Rank C.

SWD is the fourth rank of the SWS. This register is always cleared and entered with (SWC) during each clock period.

SWE is the fifth rank of the SWS. This register is always cleared and entered with (SWD) or I/O Input Data during each clock period.

SWF is the sixth rank of SWS. This register is always cleared and entered with (SWE) or LCM Read Data for an LCM to SCM block copy during each clock period.

SWG AND PARITY GENERATOR

SWG is the seventh and last rank of SWS. This circuit also generates an odd parity bit for every 12 bits in the 60-bit data word. SWG is always cleared and entered with (SWF) and the five parity bits during each clock period.

WRITE/READ RESTORE DATA SELECT

A 65-bit distribution network handles all data going to SCM Banks. This network selects either (SWG) or read restore data from the Read Merge circuit for input to all SCM Bank Inhibit Registers. Only one of the banks will enter the selected data into its Inhibit Register.

READ DATA PATHS

READ REGISTERS AND MERGE

There are eight Bank Read Registers in SCM. Each of these registers is shared by four SCM Banks. Data is transmitted to a Read Register from an SCM Bank during the read portion of the read/write cycle. Since only one SCM Bank may be initiated in any one clock period, there can be only one bank entering Read Data into a Read Register during any one clock period. The eight sets of Read Data paths from these registers are connected to a Read Merge network. This static network provides a common point for SCM Read Data from all 32 banks. The single-word output of this network is distributed to the IWS, an X Register, the SRO Register, and back to the appropriate Bank Inhibit Register for memory restoration. Only the 60 data bits are sent to the IWS and X Register. The SRO and Bank Inhibit Registers also receive the five SCM parity bits.

STORAGE READ-OUT (SRO) REGISTER

The SRO Register is used to relay SCM Read Data to other sections of the central computer. New data can enter this 65-bit register from the Read Merge network during every clock period. This register contains Read Data from the SCM Bank that has been sensed in the previous clock period. If all banks were idle, all ones enter the SRO Register. Output data from this register is sent to LCM, I/O Multiplexer, or exchange package registers.

PARITY CHECK

The data in the SRO Register is also merged in a Parity Check network. This network checks the 13 bits in each of the five fields of the 65-bit word. If no parity errors exist, each field will contain an odd number of one bits and the Parity Check network will output five zero Parity Error Bits.

PARITY ERROR REGISTER

The output of the Parity Check network is sent to the SCM Parity Error Register. Any previous error data must be cleared before new data can be entered. This register is monitored by the MCU for SCM Parity Errors. A PSD register flag is set if an SCM Parity Error has occurred.

SCM BANK

READ/WRITE CYCLE INITIATION

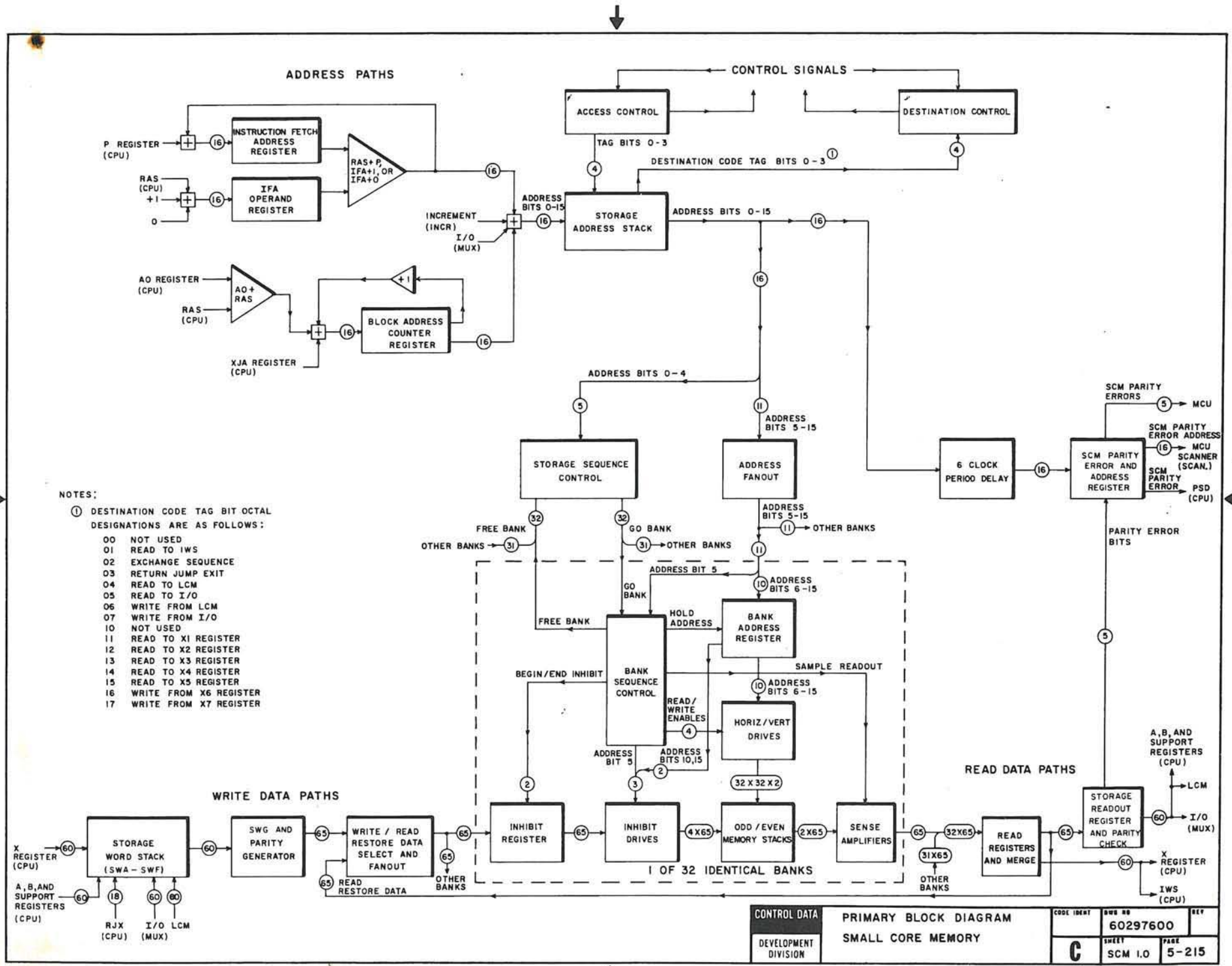
A bank read/write cycle begins when a Go Bank signal has been generated by the Storage Sequence Control. At this time, Address Bits 6-15 are entered into the Bank Address Register from the SAS. This address is held in the register until the cycle is complete.

READ/SENSE

The read portion of the bank read/write cycle begins when the Bank Sequence Control generates a Read Enable signal. Bits 6-10 of the address select the vertical drive and bits 11-15 select the horizontal drive. During the read cycle, current flows thru the selected drive lines. The resultant sense signals are amplified and gated to a Bank Read Register which is shared with three other banks. Since a read cycle destroys the selected word in memory, a write or restoration cycle follows.

WRITE/INHIBIT

The write portion of the bank read/write cycle begins when Begin Inhibit and Write Enable signals are generated by the Bank Sequence Control. Current flows thru the previously selected drive lines in the opposite direction than during the read cycle. Since unopposed write current would switch all selected cores to a one state, an inhibit current is generated when a zero state is desired. The inhibit current flows through inhibit lines which are arranged in two parallel groups of 16 lines each on each memory plane. They are vertically oriented on the even planes and horizontally oriented on the odd planes. Inhibit current is generated for the selected word by the bits that are set in the Bank Inhibit Register. This register holds the complement of write data. The inhibit current is directed to the correct stack and half-plane by a translation of Address Bits 5, 10, and 15.



NOTES:

(1) DESTINATION CODE TAG BIT OCTAL DESIGNATIONS ARE AS FOLLOWS:

00	NOT USED
01	READ TO IWS
02	EXCHANGE SEQUENCE
03	RETURN JUMP EXIT
04	READ TO LCM
05	READ TO I/O
06	WRITE FROM LCM
07	WRITE FROM I/O
10	NOT USED
11	READ TO X1 REGISTER
12	READ TO X2 REGISTER
13	READ TO X3 REGISTER
14	READ TO X4 REGISTER
15	READ TO X5 REGISTER
16	WRITE FROM X6 REGISTER
17	WRITE FROM X7 REGISTER

CONTROL DATA DEVELOPMENT DIVISION	PRIMARY BLOCK DIAGRAM SMALL CORE MEMORY	CODE IDENT	DWG NO 60297600	REV
		C	SHEET SCM 1.0	PAGE 5-215

SECONDARY BLOCK DIAGRAM
SCM ACCESS AND DESTINATION CONTROL,
WRITE DATA AND ADDRESS PATHS

SCM ACCESS CONTROL

The LM module translates control signals from other parts of the system to determine SCM address priority. This module also generates control signals which ensure that addresses and data arrive at the SCM at the proper time.

There are four sources for addresses to SCM. These are IFA Register, BAK Register, Increment Unit, and I/O Multiplexer. The IFA and BAK Registers are each used for two functions. Therefore, six basic functions require an SCM reference. The SCM Access Control determines the priority when two or more of these functions request an SCM reference in the same clock period.

Each address which enters SCM has associated with it a 4-bit destination code (tag bits). These tag bits are generated in the SCM Access Control as a result of translations of the individual access requests from other parts of the system. The SCM Access Control utilizes a delayed i designator value in forming the 4-bit tag for Increment Unit requests. This i designator value is transmitted every clock period by the X Register Access Control. The other tag values are formed as a result of translating the SCM request signals.

DESTINATION CONTROL

The 9JC7 module receives a 4-bit destination code tag from the SAS (SL module) each clock period. This code is translated to determine the destination for each address processed by the SAS (SK-1 and SK-2 modules). Control signals are then generated by the Destination Control to allow the SCM data to be entered into the selected destination register at the proper time.

STORAGE WORD STACK (SWS)

The SWS is a buffer area for 60-bit data words which are to be written into SCM. There are seven ranks of 60-bit registers in this stack. The first six ranks are contained in HM modules. The last rank is contained in HN modules.

SWA is the first rank of the SWS. This register is normally cleared and entered with (Xi) during each clock period. This data is shifted through the seven ranks of SWS and written into SCM only when an increment instruction is issued which requires an SCM reference. In all other cases the data is shifted through the ranks and discarded. This normal mode of operation is altered in the event of an SCM conflict or when an exchange sequence request is issued. An SCM conflict occurs when a bank cannot accept an address from the SAS because the previous read/write cycle for the selected bank has not been completed. In this case, the data is held in SWA until the conflict has been resolved. No conflict condition is indicated by the presence of a Shift SWA signal from the SCM Access Control (LM module). When an exchange sequence request is issued, the SCM Access Control generates a Switch SWA For Exchange signal. This signal blocks the Xi register data and allows the first eight 60-bit words of the exchange package to be shifted through the SWS into SCM. The last eight words of the exchange package consist of X register data which is shifted through the SWS in the normal mode of operation.

SWB is the second rank of the SWS. This register is normally cleared and entered with (SWA) during each clock period. This normal mode of operation is altered in the event of an SCM conflict or when a return jump instruction is issued. In the event of an SCM conflict, the data is held in SWB until the conflict has been resolved and a Shift SWB signal is generated by the SCM Access Control. When a return jump instruction is issued, the SCM Access Control generates a Switch SWB for RJX signal. This signal blocks SWA data and enters RJX from the HO module into bit positions 30-47 of SWB. The remaining bit positions of the 60-bit word become logical zeros except bit 56 which becomes logical one.

SWC is the third rank of the SWS. This register is normally cleared and entered with (SWB) during each clock period. In the event of an SCM conflict, the data is held in SWC until the conflict has been resolved and a Shift SWC signal is generated by the SCM Access Control.

When a complete memory backup occurs, data held in SWC corresponds to SAS Rank A, data held in SWB corresponds to SAS Rank B, and data held in SWA corresponds to SAS Rank C.

SWD is the fourth rank of the SWS. This register is always cleared and entered with (SWC) during each clock period.

SWE is the fifth rank of the SWS. This register is always cleared and entered with (SWD) or I/O Input Data during each clock period. I/O Input Data is entered only when a Switch SWE for I/O signal has been generated by the Destination Control (SJ module).

SWF is the sixth rank of SWS. This register is always cleared and entered with (SWE) or LCM Read Data during each clock period. LCM Read Data is entered only when a Switch SWF for LCM signal has been generated by the Destination Control.

SWG (HN modules) is the seventh and last rank of SWS. This module generates an odd parity bit for every 12 bits in the 60-bit data word. SWG is always cleared and entered with (SWF) and the five parity bits during each clock period. In the following clock period, the data and parity bits are entered into the SCM Bank Inhibit Registers (SG modules) if a Write SCM signal has been generated by the Destination Control. If this signal is not present, the information is discarded.

WRITE/READ RESTORE DATA SELECT

A 65-bit distribution network (SI modules) handles all data going to SCM Banks. This network selects either (SWG) or read restore data from the Read Data Merge (SH modules) for input to the SCM Bank Inhibit Registers (SG modules). The selection is based on the Write SCM signal generated by the Destination Control. When this signal is present, (SWG) is selected. When not present, read restore data is selected.

INSTRUCTION FETCH ADDRESS (IFA)

The IFA circuit (HI and LL modules) contains two operand selection networks, two clear/enter type operand holding registers, and a two-stage adder. The adder output is gated into the SAS (SK-1 and SK-2 modules) when a Gate IFA to SAS signal has been generated by the SCM Access Control (LM module). There are three possible outputs from the IFA adder. When either Enter IFA-1 or Enter IFA-2 signal is generated by the Coincidence Test and Fetch Translator (LO module), the adder outputs (P) + (RAS). When Advance IFA signal is generated by the SCM Access Control (LM module), the adder output increases by one from its previous value. If neither of these signals is present, the adder output remains unchanged from the previous value. If both signals are present, the adder outputs (P) + (RAS).

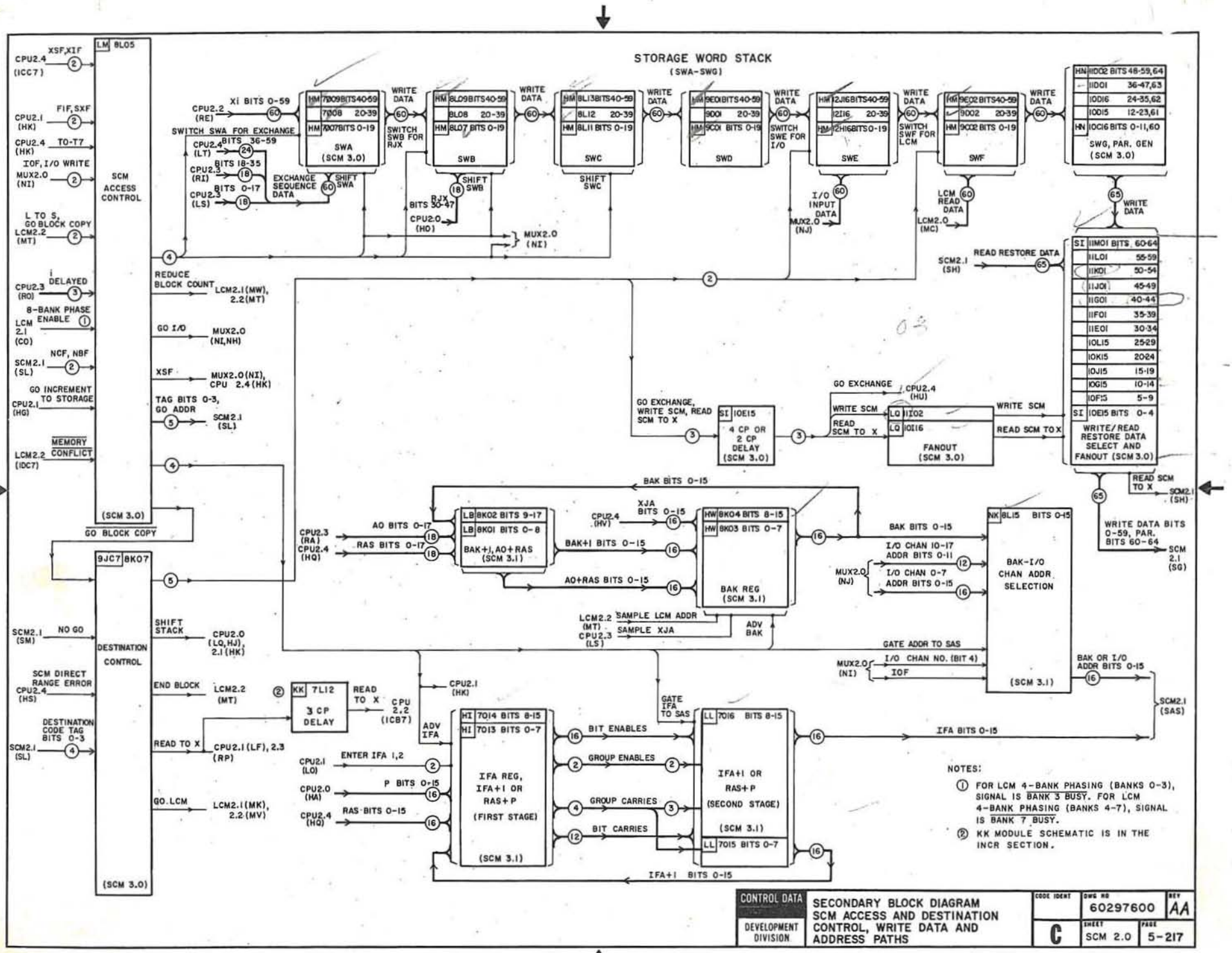
BLOCK ADDRESS COUNTER (BAK)

The BAK Register and its associated static networks form the mechanism for counting thru the 16 address values required in an exchange sequence. The initial exchange sequence address is XJA Bits 0-15 from the HV module. This address enters the BAK Register (HW modules) during a clock period in which a Sample XJA signal has been generated by the LS module. In the following clock period, this address enters the SAS (via NK module) if an IOF signal from the NI module is not present and a Gate Address to SAS signal has been generated by the SCM Access Control (LM module). The address value is incremented by one as each address is entered into the SAS. The incrementing is performed by the LB module and is continued until all 16 addresses have been entered in the SAS. This process is controlled by the Advance BAK signal from the LM module.

The BAK Register and its associated static networks also form the mechanism for counting thru all of the addresses in an SCM to LCM or LCM to SCM block copy. The initial address is A0 + RAS Bits 0-15. This address is formed by the LB modules and enters the BAK Register (HW modules) during a clock period in which a Sample LCM Address signal has been generated by the MT module. In the following clock period, this address enters the SAS (via NK module) if an IOF signal from the NI module is not present and a Gate Address to SAS signal has been generated by the SCM Access Control (LM module). The address value is incremented by one as each address is entered into the SAS. The incrementing is performed by the LB module and is continued until all block copy addresses have been entered in the SAS. This process is controlled by the Advance BAK signal from the LM module.

I/O ADDRESSES

Addresses from the I/O Multiplexer are entered into the SAS from the NK module whenever an IOF signal is generated by the NI module and a Gate Address to SAS signal is generated by the SCM Access Control (LM module). I/O Channel 10-17 Address is selected if bit 4 of the I/O Channel Priority No. is set. If bit 4 is not set, I/O Channel 0-7 Address is selected. All addresses are treated as 16-bit quantities. I/O Channel 10-17, which contains only 12 bits, is extended with four higher order zero bits.


STORAGE WORD STACK
(SWA-SWG)
SCM ACCESS CONTROL
(SCM 3.0)
DESTINATION CONTROL
(SCM 3.0)
SWA (SCM 3.0)
SWB
SWC
SWD
SWE
SWF
SWG, PAR. GEN (SCM 3.0)
WRITE/READ RESTORE DATA SELECT AND FANOUT (SCM 3.0)
4 CP OR 2 CP DELAY (SCM 3.0)
FANOUT (SCM 3.0)
BAK REG (SCM 3.1)
BAK-I/O CHAN ADDR SELECTION (SCM 3.1)
IFA REG, IFA+1 OR RAS+P (FIRST STAGE) (SCM 3.1)
IFA+1 OR RAS+P (SECOND STAGE) (SCM 3.1)
3 CP DELAY
NOTES:
① FOR LCM 4-BANK PHASING (BANKS 0-3), SIGNAL IS BANK 3 BUSY. FOR LCM 4-BANK PHASING (BANKS 4-7), SIGNAL IS BANK 7 BUSY.
② KK MODULE SCHEMATIC IS IN THE INCR SECTION.
CONTROL DATA
DEVELOPMENT DIVISION
SECONDARY BLOCK DIAGRAM
SCM ACCESS AND DESTINATION CONTROL, WRITE DATA AND ADDRESS PATHS
CODE IDENT
C
DWG NO
60297600
REV
AA
SHEET
SCM 2.0
PAGE
5-217

SECONDARY BLOCK DIAGRAM
SCM BANKS AND DISTRIBUTION, ADDRESS PATHS,
AND READ DATA PATHS

STORAGE ADDRESS STACK (SAS)

The SAS is a holding area for addresses arriving at the SCM. There are three 20-bit registers in the SAS which are referred to as Rank A, Rank B, and Rank C. These registers hold a 16-bit SCM address (SK-1 and SK-2 modules) and a four-bit destination code (SL module). The Destination Code Tag Bits are sent to the Destination Control (9JC7 module) where they are interpreted.

If no SCM bank conflicts occur (No Go signal not present from SM module), an address enters SAS Rank A in any given clock period and leaves in the following clock period. SAS Ranks B and C are not involved even if a new address enters Rank A every clock period. When a conflict occurs (No Go signal present), the address in Rank A is held until the conflict is resolved. If another address arrives at the SAS during this time, it will enter Rank B. When this occurs, no more addresses will be issued to the SAS until the backup condition has been resolved. There may be one address being processed in the Increment Unit at this time. If so, this address will enter Rank C. When a conflict has caused a backup situation in the SAS, no new addresses will be accepted until all previously entered addresses have left the SAS. The addresses leave the SAS in the same order in which they entered.

Address Bits 0-15 leave the SAS and arrive at the Parity Error Address Register (HT module) after a delay of six clock periods. This delay is accomplished by SI modules. Address Bits 5-15 are sent from the SAS to all SCM Banks. The fanout to the 32 SCM Banks is accomplished by LQ modules. Address Bits 0-4 are sent from the SAS to the Bank Select Translator (SM modules).

STORAGE CONFLICT CONTROL AND BANK SELECT

The lower five address bits determine which of the 32 SCM Banks has been selected for a read/write cycle. The selected bank will receive a Go Bank signal from the SM module if an Address Flag signal has been generated by the SL module, and a Bank Busy signal has been generated by the SN module. The Bank Busy signal is dependent on the selected bank's Bank Busy Flag being clear, indicating that the previous read/write cycle has been completed.

SCM BANKS AND DISTRIBUTION

INHIBIT REGISTERS

Each SCM Bank has a 65-bit Bank Inhibit Register (SG modules). Each SG module contains five bits of the registers for four banks. Write Data Bits 0-59 and Parity Bits 60-64 from the SI module are present at the input of all Bank Inhibit Registers. This data is complemented and gated into the register that has a Begin Inhibit signal present from the selected bank. The Inhibit Data remains in the register until an End Inhibit signal from the selected bank is generated.

SCM BANKS

There are 32 identical memory banks in SCM. Each SCM Bank contains ten 9SA7 modules, five 2SB7 mdoules, five 2SC7 modules, two SD modules, one SE module, and one SF module. The 9SA7 modules each contain a memory stack plus the associated read/write drive circuits. All 65-bit (including parity) words with address bit 5 equal to zero are stored in five even stacks. All words with address bit 5 equal to one are stored in five odd stacks. The 2SB7 and 2SC7 modules are similar to each other in that each contains part of the inhibit and sense circuits. The SD modules contain the Bank Address Register. This register contains address bits 6-15 which are fanned-out to each 9SA7 module. The SE module contains the Bank Sequence Control. The SF module contains a fanout for address bits 5, 10, and 15 to the 2SB7 and 2SC7 modules and Begin/End Inhibit signals to the Bank Inhibit Registers (SG modules).

FOUR-BANK READ MERGE AND REGISTERS

There are eight Bank Read Registers (SG modules) in SCM. Each of these register is shared by four SCM Banks. The SG modules each contain five bits of the common register for four banks. Read Data is transmitted to a Read Register from an SCM Bank during the read portion of the read/write cycle. Since only one SCM Bank may be initiated in any one clock period, there can be only one bank entering Read Data into a Read Register every clock period.

READ DATA MERGE

The eight sets of Read Data paths from these registers are connected to a Read Data Merge network in the SH modules. This static network provides a common point for SCM Read Data from all 32 banks. The single-word output of this network is distributed to the IWS, an X Register, the SRO Register, and back to the appropriate Bank Inhibit Register (thru SI modules) for memory restoration. Read Data output to an X Register is dependent on a Read SCM to X control signal from the SI module. Only the 60 data bits are sent to the IWS and X Register. The SRO and Bank Inhibit Registers receive the five SCM parity bits as well as the 60 data bits.

STORAGE READ-OUT (SRO) REGISTER

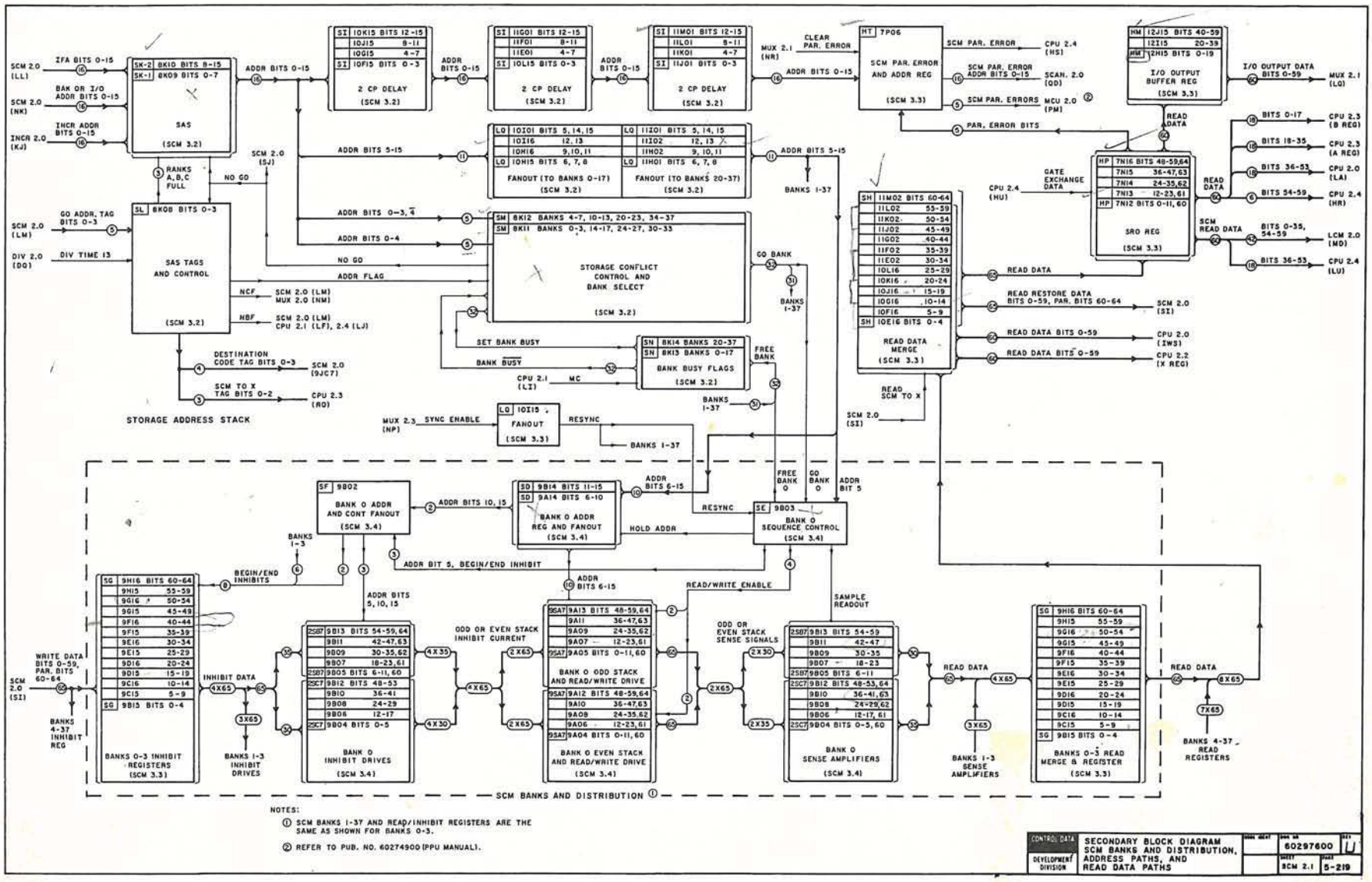
The SRO Register (HP modules) is used to relay SCM Read Data to other sections of the central computer. New data enters this 65-bit register from the Read Data Merge network (SH modules) during every clock period. This register contains Read Data from the SCM Bank that has been sensed in the previous clock period. If all banks were idle, all ones enter the SRO Register. Output data from this register is sent to LCM, I/O Multiplexer, or exchange package registers. The data is gated at the receiving end of these transmission paths. However, data sent to the A and B Registers during an exchange sequence is dependent on a Gate Exchange Data signal from the HU module. Data sent to the I/O Multiplexer is first entered into an I/O Output Buffer Register (HM modules).

The data in the SRO Register is also merged in a Parity Check network (HP modules). This network checks the 13 bits in each of the five fields of the 65-bit word. If no parity errors exist, each field will contain an odd number of one bits and the Parity Check network will output five zero Parity Error Bits. If a parity error has occurred, the corresponding field will contain an even number of one bits and the Parity Check network will output a one and four zero Parity Error Bits.

SCM PARITY ERROR AND ADDRESS REGISTERS

The output of the Parity Check network is sent to the SCM Parity Error Register (HT module). Any previous error data must be cleared before new data can be entered. This register is monitored by the MCU (PM module) for SCM Parity Errors. A PSD register (HS module) Flag is set if an SCM Parity Error has occurred.

The error address is held in the SCM Parity Error Address Register (HT module). This register is monitored by the MCU Scanner (QD modules). SCM addresses are entered into this register every clock period if none of the SCM Parity Error Register bits are ones. When a parity error does occur, one or more of these bits will be a one. This blocks entry of any subsequent addresses in the SCM Pairyt Error Address Register. The SCM address at which the parity error occurred is held in the register.


SCM 2.0 (LL)
IFA BITS 0-15
BAK OR I/O ADDR BITS 0-15
SCM 2.0 (NK)
INCR ADDR BITS 0-15
INCR 2.0 (KJ)
SAS (SCM 3.2)
ADDR BITS 0-15
2 CP DELAY (SCM 3.2)
MUX 2.1 (NR)
CLEAR PAR. ERROR
SCM PAR. ERROR AND ADDR REG (SCM 3.3)
SCM PAR. ERROR
CPU 2.4 (HS)
SCM PAR. ERROR ADDR BITS 0-15
SCAN. 2.0 (QD)
SCM PAR. ERRORS
MCU 2.0 (PM)
I/O OUTPUT BUFFER REG (SCM 3.3)
I/O OUTPUT DATA BITS 0-59
MUX 2.1 (LQ)
PAR. ERROR BITS
READ DATA
BITS 0-17
CPU 2.3 (B REG)
BITS 18-35
CPU 2.3 (A REG)
BITS 36-53
CPU 2.0 (LA)
BITS 54-59
CPU 2.4 (HR)
RANKS A,B,C FULL
NO GO
SCM 2.0 (SJ)
ADDR BITS 5-15
BANKS 1-37
GATE EXCHANGE DATA
CPU 2.4 (HU)
SRO REG (SCM 3.3)
SCM READ DATA
BITS 0-35, 54-59
LCM 2.0 (MD)
BITS 36-53
CPU 2.4 (LU)
GO ADDR, TAG BITS 0-3
SCM 2.0 (LM)
DIV 2.0 (DQ)
DIV TIME 13
SAS TAGS AND CONTROL (SCM 3.2)
ADDR BITS 0-3, 4
ADDR BITS 0-4
ADDR FLAG
NCF
SCM 2.0 (LM) MUX 2.0 (NM)
NBF
SCM 2.0 (LM) CPU 2.1 (LF), 2.4 (LJ)
STORAGE CONFLICT CONTROL AND BANK SELECT (SCM 3.2)
GO BANK
SET BANK BUSY
BANK BUSY
CPU 2.1 (LI)
MC
BANK BUSY FLAGS (SCM 3.2)
FREE BANK
READ DATA MERGE (SCM 3.3)
READ DATA
READ RESTORE DATA BITS 0-59, PAR. BITS 60-64
SCM 2.0 (SI)
READ DATA BITS 0-59
CPU 2.0 (IWS)
CPU 2.2 (X REG)
READ SCM TO X
DESTINATION CODE TAG BITS 0-3
SCM 2.0 (9JC7)
SCM TO X TAG BITS 0-2
CPU 2.3 (RO)
STORAGE ADDRESS STACK
MUX 2.3 (NP)
SYNC ENABLE
FANOUT (SCM 3.3)
RESYNC
BANK 0 ADDR AND CONT FANOUT (SCM 3.4)
BANK 0 ADDR REG AND FANOUT (SCM 3.4)
ADDR BITS 6-15
ADDR BITS 10, 15
HOLD ADDR
BANK 0 SEQUENCE CONTROL (SCM 3.4)
FREE BANK 0
GO BANK 0
ADDR BIT 5
BANKS 1-3
BEGIN/END INHIBITS
ADDR BIT 5, BEGIN/END INHIBIT
READ/WRITE ENABLE
SAMPLE READOUT
ADDR BITS 5, 10, 15
WRITE DATA BITS 0-59, PAR. BITS 60-64
INHIBIT DATA
BANKS 0-3 INHIBIT REGISTERS (SCM 3.3)
BANKS 4-37 INHIBIT REG
BANKS 1-3 INHIBIT DRIVES
BANK 0 INHIBIT DRIVES (SCM 3.4)
ODD OR EVEN STACK INHIBIT CURRENT
BANK 0 ODD STACK AND READ/WRITE DRIVE
BANK 0 EVEN STACK AND READ/WRITE DRIVE
ODD OR EVEN STACK SENSE SIGNALS
BANK 0 SENSE AMPLIFIERS (SCM 3.4)
BANKS 1-3 SENSE AMPLIFIERS
BANKS 0-3 READ MERGE & REGISTER (SCM 3.3)
BANKS 4-37 READ REGISTERS
SCM BANKS AND DISTRIBUTION ①
NOTES:
① SCM BANKS 1-37 AND READ/INHIBIT REGISTERS ARE THE SAME AS SHOWN FOR BANKS 0-3.
② REFER TO PUB. NO. 60274900 (PPU MANUAL).
CONTROL DATA DEVELOPMENT DIVISION
SECONDARY BLOCK DIAGRAM SCM BANKS AND DISTRIBUTION, ADDRESS PATHS, AND READ DATA PATHS
60297600
SCM 2.1
5-219

DETAILED-MODULES DIAGRAM
SCM ACCESS CONTROL, DESTINATION CONTROL,
AND WRITE DATA PATHS

SCM ACCESS CONTROL

The LM module translates control signals from other parts of the system to determine SCM address priority. This module also generates control signals which ensure that addresses and data arrive at the SCM at the proper time.

ADDRESS SELECTION

There are four sources for addresses to SCM. These are IFA Register, BAK Register, Increment Unit, and I/O Multiplexer. The IFA and BAK Registers are each used for two functions. Therefore, six basic functions require an SCM reference. The SCM Access Control determines the priority when two or more of these functions request an SCM reference in the same clock period. Only one address may be accepted in a given clock period, and the choice is dictated by the following priority list:

1. Exchange sequence request (BAK Register)
2. Increment Unit request
3. Return jump exit request (IFA Register)
4. I/O Multiplexer request
5. Instruction fetch request (IFA Register)
6. LCM block copy request (BAK Register)

ADDRESS TAGS

Each address which enters SCM has associated with it a 4-bit destination code (tag bits). These tag bits are generated in the SCM Access Control as a result of translations of the individual access requests from other parts of the system. The SCM Access Control utilizes a delayed i designator value in forming the 4-bit tag for Increment Unit requests. This i designator value is transmitted every clock period by the X Register Access Control. The other tag values are formed as a result of translating the SCM request signals. The octal values for these tag bits are as follows:

00	Not Used	10	Not Used
01	Read to IWS	11	Read to X1 Register
02	Exchange sequence	12	Read to X2 Register
03	Return jump exit	13	Read to X3 Register
04	Read SCM to LCM	14	Read to X4 Register
05	Read SCM to MUX	15	Read to X5 Register
06	Write LCM to SCM	16	Write from X6 Register
07	Write MUX to SCM	17	Write from X7 Register

DESTINATION CONTROL

The 9JC7 module receives a 4-bit destination code tag from the SAS (SL module) each clock period. This code is translated to determine the destination for each address processed by the SAS (SK-1 and SK-2 modules). Control signals are then generated by the Destination Control to allow the SCM data to be entered into the selected destination register at the proper time.

WRITE DATA PATHS

STORAGE WORD STACK (SWS)

The SWS is a buffer area for 60-bit data words which are to be written into SCM. There are seven ranks of 60-bit registers in this stack. The first six ranks are contained in HM modules. The last rank is contained in HN modules.

Storage Word Stack Rank A (SWA)

SWA is the first rank of the SWS. This register is normally cleared and entered with (Xi) during each clock period. This data is shifted through the seven ranks of SWS and written into SCM only when an increment instruction is issued which requires an SCM reference. In all other cases the data is shifted through the ranks and discarded. This normal mode of operation is altered in the event of an SCM conflict or when an exchange sequence request is issued.

An SCM conflict occurs when a bank cannot accept an address from the SAS because the previous read/write cycle for the bank has not been completed. In this case, the data is held in SWA until the conflict has been resolved. This is indicated by the presence of a Shift SWA signal from the SCM Access Control (LM module).

When an exchange sequence request is issued, the SCM Access Control generates a Switch SWA For Exchange signal. This signal blocks the Xi register data and allows the first eight 60-bit words of the exchange package to be shifted through the SWS into SCM. The last eight words of the exchange package consist of X register data which is shifted through the SWS in the normal mode of operation.

Storage Word Stack Rank B (SWB)

SWB is the second rank of the SWS. This register is normally cleared and entered with (SWA) during each clock period. This normal mode of operation is altered in the event of an SCM conflict or when a return jump instruction is issued.

In the event of an SCM conflict, the data is held in SWB until the conflict has been resolved and a Shift SWB signal is generated by the SCM Access Control.

When a return jump instruction is issued, the SCM Access Control generates a Switch SWB for RJX signal. This signal blocks SWA data and enters RJX from the HO module into bit positions 30-47 of SWB. The remaining bit positions of the 60-bit word become logical zeros except bit 56 which becomes logical one.

Storage Word Stack Rank C (SWC)

SWC is the third rank of the SWS. This register is normally cleared and entered with (SWB) during each clock period. In the event of an SCM conflict, the data is held in SWC until the conflict has been resolved and a Shift SWC signal is generated by the SCM Access Control.

Storage Word Stack Rank D (SWD)

SWD is the fourth rank of the SWS. This register is always cleared and entered with (SWC) during each clock period.

Storage Word Stack Rank E (SWE)

SWE is the fifth rank of the SWS. This register is always cleared and entered with (SWD) or I/O Input Data during each clock period. I/O Input Data is entered only when a Switch SWE for I/O signal has been generated by the Destination Control (SJ module).

Storage Word Stack Rank F (SWF)

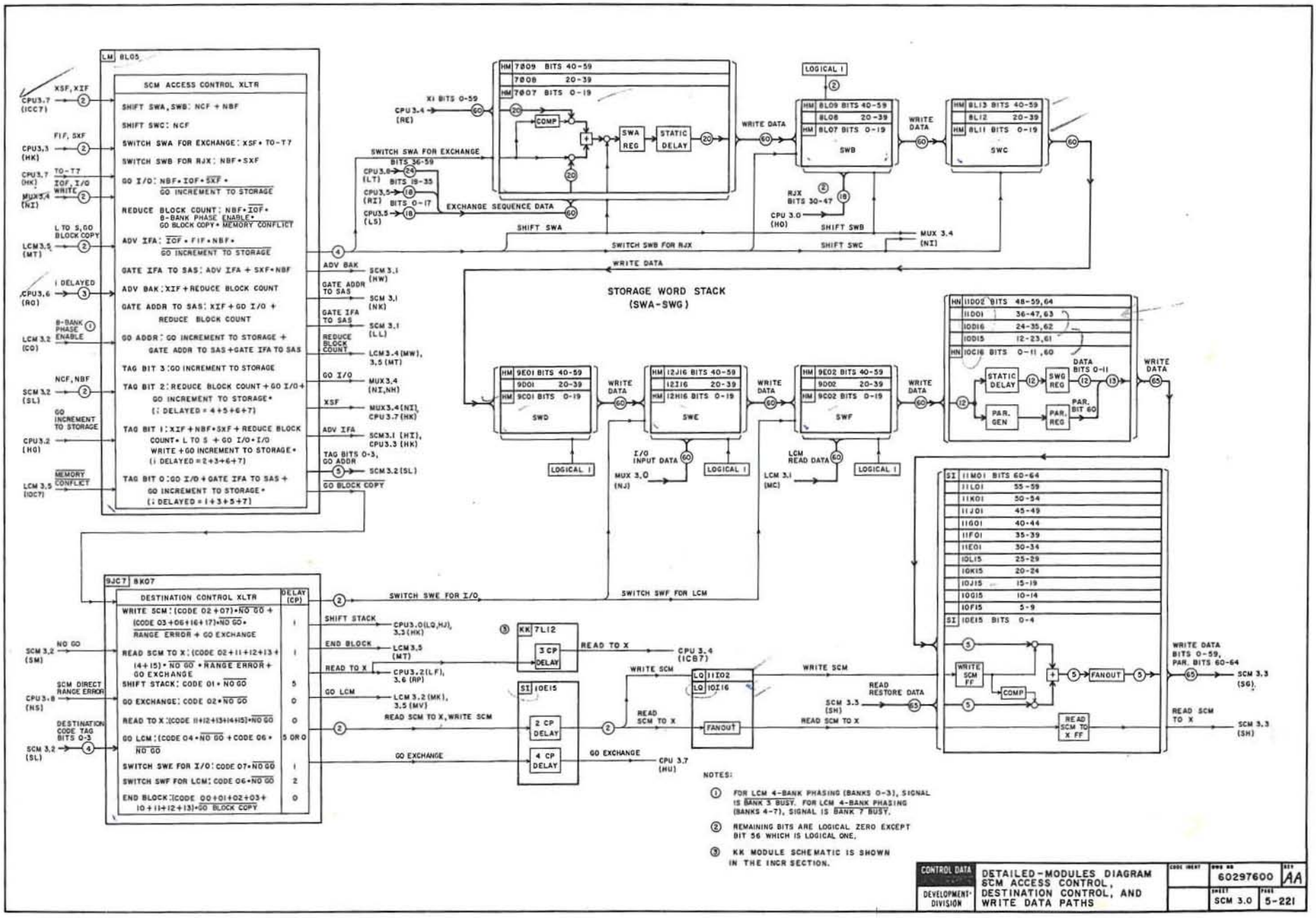
SWF is the sixth rank of SWS. This register is always cleared and entered with (SWE) or LCM Read Data during each clock period. LCM Read Data is entered only when a Switch SWF for LCM signal has been generated by the Destination Control.

Storage Word Stack Rank G (SWG)

SWG (HN modules) is the seventh and last rank of SWS. This module generates an odd parity bit for every 12 bits in the 60-bit data word. SWG is always cleared and entered with (SWF) and the five parity bits during each clock period. In the following clock period, the data and parity bits are entered into the SCM Bank Inhibit Registers (SG modules) if a Write SCM signal has been generated by the Destination Control. If this signal is not present, the information is discarded.

WRITE/READ RESTORE DATA SELECT

A 65-bit distribution network (SI modules) handles all data going to SCM Banks. This network selects either (SWG) or read restore data from the Read Data Merge (SH modules) for input to the SCM Bank Inhibit Registers (SG modules). The selection is based on the Write SCM signal generated by the Destination Control. When this signal is present, (SWG) is selected. When not present, read restore data is selected.


LM 8L05
SCM ACCESS CONTROL XLTR
SHIFT SWA, SWB: NCF + NBF
SHIFT SWC: NCF
SWITCH SWA FOR EXCHANGE: XSF • T0-T7
SWITCH SWB FOR RJX: NBF • SXF
GO I/O: NBF • IOF • SXF • GO INCREMENT TO STORAGE
REDUCE BLOCK COUNT: NBF • IOF • 8-BANK PHASE ENABLE • GO BLOCK COPY • MEMORY CONFLICT
ADV IFA: IOF • FIF • NBF • GO INCREMENT TO STORAGE
GATE IFA TO SAS: ADV IFA + SXF • NBF
ADV BAK: XIF + REDUCE BLOCK COUNT
GATE ADDR TO SAS: XIF + GO I/O + REDUCE BLOCK COUNT
GO ADDR: GO INCREMENT TO STORAGE + GATE ADDR TO SAS + GATE IFA TO SAS
TAG BIT 3: GO INCREMENT TO STORAGE
TAG BIT 2: REDUCE BLOCK COUNT + GO I/O + GO INCREMENT TO STORAGE • (↓ DELAYED = 4+5+6+7)
TAG BIT 1: XIF + NBF + SXF + REDUCE BLOCK COUNT • L TO S + GO I/O • I/O WRITE + GO INCREMENT TO STORAGE • (↓ DELAYED = 2+3+6+7)
TAG BIT 0: GO I/O + GATE IFA TO SAS + GO INCREMENT TO STORAGE • (↓ DELAYED = 1+3+5+7)
XSF, XIF
CPU3.7 (ICC7)
FIF, SXF
CPU3.3 (HK)
T0-T7
CPU3.7 (HK)
IOF, I/O WRITE
MUX3.4 (NI)
L TO S, GO BLOCK COPY
LCM3.5 (MT)
↓ DELAYED
CPU3.6 (RG)
8-BANK PHASE ENABLE
LCM3.2 (CG)
NCF, NBF
SCM3.2 (SL)
GO INCREMENT TO STORAGE
CPU3.2 (HG)
MEMORY CONFLICT
LCM3.5 (IOC7)
ADV BAK
SCM3.1 (HW)
GATE ADDR TO SAS
SCM3.1 (NK)
GATE IFA TO SAS
SCM3.1 (LL)
REDUCE BLOCK COUNT
LCM3.4 (MW), 3.5 (MT)
GO I/O
MUX3.4 (NI,NK)
XSF
MUX3.4 (NI), CPU3.7 (HK)
ADV IFA
SCM3.1 (HI), CPU3.3 (HK)
TAG BITS 0-3, GO ADDR
SCM3.2 (SL)
GO BLOCK COPY
SWITCH SWA FOR EXCHANGE BITS 36-59
CPU3.0 (LT) BITS 18-35
CPU3.5 (RI) BITS 0-17
CPU3.5 (LS)
EXCHANGE SEQUENCE DATA
XI BITS 0-59
CPU3.4 (RE)
HM 7809 BITS 40-59
7808 20-39
HM 7807 BITS 0-19
COMP
SWA REG
STATIC DELAY
WRITE DATA
LOGICAL 1
HM 8L09 BITS 40-59
8L08 20-39
HM 8L07 BITS 0-19
SWB
HM 8L13 BITS 40-59
8L12 20-39
HM 8L11 BITS 0-19
SWC
RJX BITS 30-47
CPU 3.0 (HO)
SHIFT SWA
SHIFT SWB
SHIFT SWC
SWITCH SWB FOR RJX
MUX 3.4 (NI)
STORAGE WORD STACK (SWA-SWG)
HM 9E01 BITS 40-59
9D01 20-39
HM 9C01 BITS 0-19
SWD
HM 12J16 BITS 40-59
12J16 20-39
HM 12H16 BITS 0-19
SWE
HM 9E02 BITS 40-59
9D02 20-39
HM 9C02 BITS 0-19
SWF
HN 11D02 BITS 48-59,64
11D01 36-47,63
10DI6 24-35,62
10DI5 12-23,61
HN 10CI6 BITS 0-11,60
STATIC DELAY
SWG REG
DATA BITS 0-11
PAR. GEN
PAR. REG
PAR. BIT 60
WRITE DATA
I/O INPUT DATA
MUX 3.0 (NJ)
LCM READ DATA
LCM 3.1 (MC)
SI 11M01 BITS 60-64
11L01 55-59
11K01 50-54
11J01 45-49
11G01 40-44
11F01 35-39
11E01 30-34
10L15 25-29
10K15 20-24
10J15 15-19
10G15 10-14
10F15 5-9
SI 10E15 BITS 0-4
WRITE SCM FF
COMP
FANOUT
WRITE DATA BITS 0-59, PAR. BITS 60-64
SCM 3.3 (SG)
READ SCM TO X FF
READ SCM TO X
SCM 3.3 (SH)
READ RESTORE DATA
WRITE SCM
READ SCM TO X
SWITCH SWE FOR I/O
SWITCH SWF FOR LCM
9JC7 8K07
DESTINATION CONTROL XLTR
DELAY (CP)
WRITE SCM: (CODE 02+07) • NO GO + (CODE 03+06+16+17) • NO GO • RANGE ERROR + GO EXCHANGE — 1
READ SCM TO X: (CODE 02+11+12+13+14+15) • NO GO + RANGE ERROR + GO EXCHANGE — 1
SHIFT STACK: CODE 01 • NO GO — 5
GO EXCHANGE: CODE 02 • NO GO — 0
READ TO X: (CODE 11+12+13+14+15) • NO GO — 0
GO LCM: (CODE 04 • NO GO + CODE 06 • NO GO — 5 OR 0
SWITCH SWE FOR I/O: CODE 07 • NO GO — 1
SWITCH SWF FOR LCM: CODE 06 • NO GO — 2
END BLOCK: (CODE 00+01+02+03+10+11+12+13) • GO BLOCK COPY — 0
NO GO
SCM 3.2 (SM)
SCM DIRECT RANGE ERROR
CPU3.8 (NS)
DESTINATION CODE TAG BITS 0-3
SCM 3.2 (SL)
SHIFT STACK
CPU3.0 (LQ,MJ), 3.3 (HK)
END BLOCK
LCM3.5 (MT)
READ TO X
CPU3.2 (LF), 3.6 (RP)
GO LCM
LCM 3.2 (MK), 3.5 (MV)
READ SCM TO X, WRITE SCM
GO EXCHANGE
CPU 3.7 (HU)
KK 7L12
3 CP DELAY
READ TO X
CPU 3.4 (ICB7)
SI 10E15
2 CP DELAY
4 CP DELAY
WRITE SCM
READ SCM TO X
LQ 11I02
LQ 10I16
FANOUT
GO EXCHANGE
NOTES:
① FOR LCM 4-BANK PHASING (BANKS 0-3), SIGNAL IS BANK 3 BUSY. FOR LCM 4-BANK PHASING (BANKS 4-7), SIGNAL IS BANK 7 BUSY.
② REMAINING BITS ARE LOGICAL ZERO EXCEPT BIT 56 WHICH IS LOGICAL ONE.
③ KK MODULE SCHEMATIC IS SHOWN IN THE INCR SECTION.
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM
SCM ACCESS CONTROL, DESTINATION CONTROL, AND WRITE DATA PATHS
CODE IDENT
60297600
REV AA
SHEET SCM 3.0
PAGE 5-221

The SAS receives addresses from four sources. These are IFA, BAK, I/O Multiplexer, and Increment Unit (INCR 3.0).

INSTRUCTION FETCH ADDRESS (IFA)

The IFA circuit (HI and LL modules) contains two operand selection networks, two clear/enter type operand holding registers, and a two-stage adder. The adder output is gated into the SAS (SK-1 and SK-2 modules) when a Gate IFA to SAS signal has been generated by the SCM Access Control (LM module). There are three possible outputs from the IFA adder. When either Enter IFA-1 or Enter IFA-2 signals is generated by the Coincidence Test and Fetch Translator (LO module), the adder outputs (P) + (RAS). When Advance IFA signal is generated by the SCM Access Control (LM module), the adder output increases by one from its previous value. If neither of these signals is present, the adder output remains unchanged from the previous value. If both signals are present, the adder outputs (P) + (RAS).

BLOCK ADDRESS COUNTER (BAK)

The BAK circuit (LB, HW, and NK modules) provides addresses for the SAS during exchange jump sequences and LCM block copies.

EXCHANGE SEQUENCE ADDRESSES

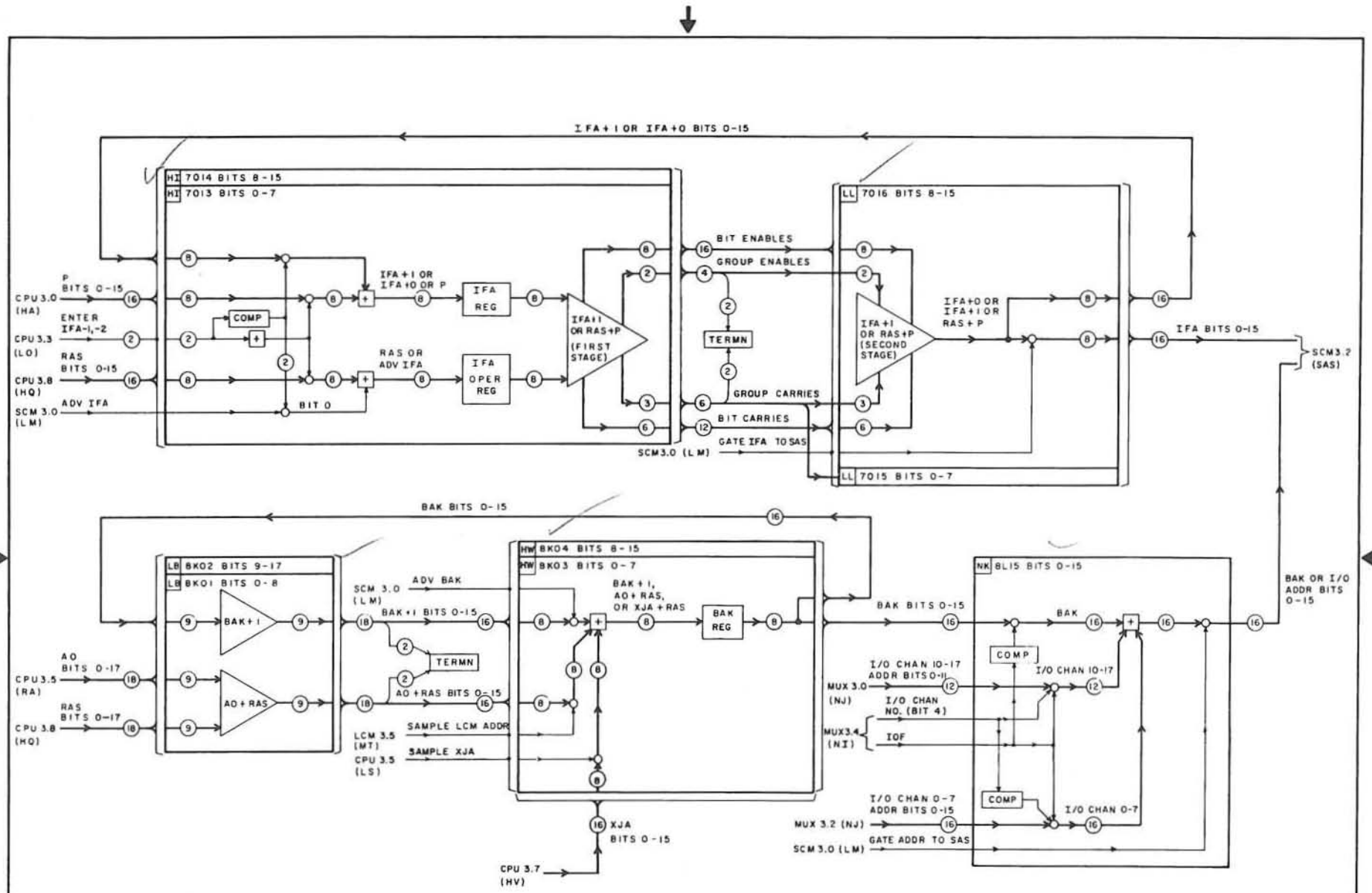
The BAK Register and its associated static networks form the mechanism for counting thru the 16 address values required in an exchange sequence. The initial exchange sequence address is XJA Bits 0-15 from the HV module. This address enters the BAK Register (HW modules) during a clock period in which a Sample XJA signal has been generated by the LS module. In the following clock period, this address enters the SAS (SK-1 and SK-2 modules) if an IOF signal from the NI module is not present and a Gate Address to SAS signal has been generated by the SCM Access Control (LM module). The address value is incremented by one as each address is entered into the SAS. The incrementing is performed by the LB module and is continued until all 16 addresses have been entered in the SAS. This process is controlled by the Advance BAK signal from the LM module.

LCM BLOCK COPY ADDRESSES

The BAK Register and its associated static networks form the mechanism for counting thru all of the addresses in an SCM to LCM or LCM to SCM block copy. The initial address is A0 + RAS Bits 0-15. This address is formed by the LB modules and enters the BAK Register (HW modules) during a clock period in which a Sample LCM Address signal has been generated by the MT module. In the following clock period, this address enters the SAS (SK-1 and SK-2 modules) if an IOF signal from the NI module is not present and a Gate Address To SAS signal has been generated by the SCM Access Control (LM module). The address value is incremented by one as each address is entered into the SAS. The incrementing is performed by the LB module and is continued until all block copy addresses have been entered in the SAS. This process is controlled by the Advance BAK signal from the LM module.

I/O ADDRESSES

Addresses from the I/O Multiplexer are entered into the SAS whenever an IOF signal is generated by the NI module and a Gate Address to SAS signal is generated by the SCM Access Control (LM module). I/O Channel 10-17 Address is selected if bit 4 of the I/O Channel Priority No. is set. If bit 4 is not set, I/O Channel 0-7 Address is selected. All addresses are treated as 16-bit quantities. I/O Channel 10-17, which contains only 12 bits, is extended with four higher order zero bits.



CONTROL DATA	DETAILED – MODULES DIAGRAM ADDRESS PATHS TO STORAGE ADDRESS STACK	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	M
		SHEET SCM 3.1	PAGE 5-223	

STORAGE ADDRESS STACK (SAS)

The SAS is a holding area for addresses arriving at the SCM. There are three 20-bit registers in the SAS which are referred to as Rank A, Rank B, and Rank C. These registers hold a 16-bit SCM address (SK-1 and SK-2 modules) and a four-bit destination code (SL module). The Destination Code Tag Bits are sent to the Destination Control (9JC7 module) where they are interpreted.

If no SCM bank conflicts occur (No Go signal not present from SM module), an address enters SAS Rank A in any given clock period and leaves in the following clock period. SAS Ranks B and C are not involved even if a new address enters Rank A every clock period.

When an SCM bank conflict occurs (No Go signal present), the address in Rank A is held until the conflict is resolved. This may be anywhere from one to nine clock periods. If another address arrives at the SAS during this period, it will enter Rank B. When this occurs, no more addresses will be issued to the SAS until the backup condition has been resolved. There may be one address being processed in the Increment Unit at this time. If so, this address will enter Rank C in the following clock period.

When an SCM bank conflict has caused a backup situation in the SAS, no new addresses will be accepted until all previously entered addresses have left the SAS. The addresses leave the SAS in the same order in which they entered. (Rank A leaves first, Rank B leaves second, and Rank C leaves last).

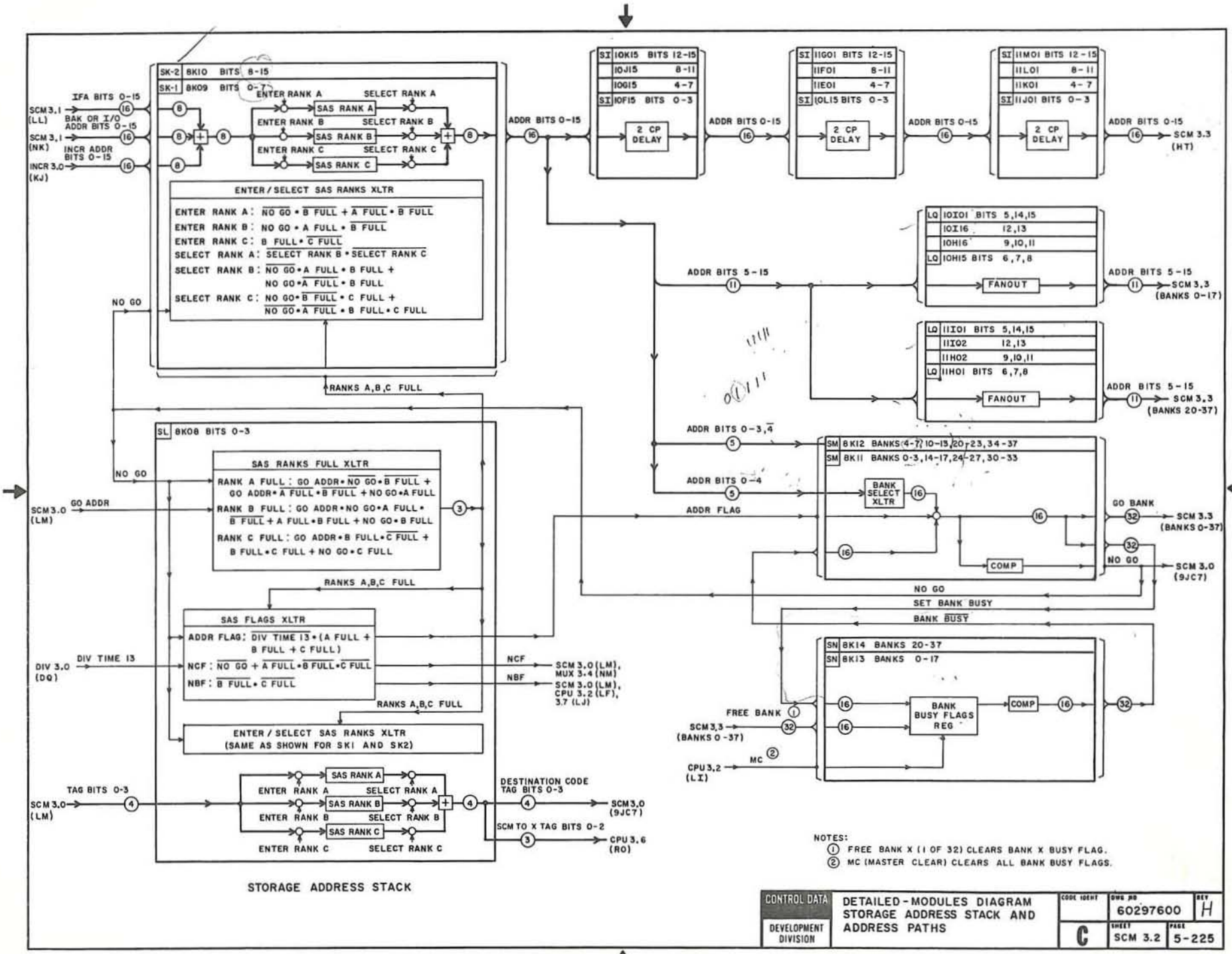
ADDRESS PATHS

Address Bits 0-15 leave the SAS and arrive at the Parity Error Address Register (HT module) after a delay of six clock periods. This delay is accomplished by SI modules.

Address Bits 5-15 are sent from the SAS to all SCM Banks. The fanout to the 32 SCM Banks is accomplished by LQ modules.

Address Bits 0-4 are sent from the SAS to the Bank Select Translator (SM modules). These lower five address bits determine which of the 32 SCM Banks has been selected for a read/write cycle. The selected bank will receive a Go Bank signal from the SM module if an Address Flag signal has been generated by the SL module, and a Bank Busy signal has been generated by the SN module. The Bank Busy signal is dependent on a Free Bank signal from the selected bank, indicating that the previous read/write cycle has been completed.

0 000 000 000 000 000


SK-2 8K10 BITS 8-15
SK-1 8K09 BITS 0-7
IFA BITS 0-15
SCM 3,1 (LL)
BAK OR I/O ADDR BITS 0-15
SCM 3,1 (NK)
INCR ADDR BITS 0-15
INCR 3,0 (KJ)
ENTER RANK A
SELECT RANK A
SAS RANK A
ENTER RANK B
SELECT RANK B
SAS RANK B
ENTER RANK C
SELECT RANK C
SAS RANK C
ENTER / SELECT SAS RANKS XLTR
ENTER RANK A: NO GO • B FULL + A FULL • B FULL
ENTER RANK B: NO GO • A FULL • B FULL
ENTER RANK C: B FULL • C FULL
SELECT RANK A: SELECT RANK B • SELECT RANK C
SELECT RANK B: NO GO • A FULL • B FULL + NO GO • A FULL • B FULL
SELECT RANK C: NO GO • B FULL • C FULL + NO GO • A FULL • B FULL • C FULL
NO GO
RANKS A,B,C FULL
ADDR BITS 0-15
SI 10K15 BITS 12-15
10J15 8-11
10G15 4-7
SI 10F15 BITS 0-3
2 CP DELAY
SI 11G01 BITS 12-15
11F01 8-11
11E01 4-7
SI 10L15 BITS 0-3
SI 11M01 BITS 12-15
11L01 8-11
11K01 4-7
SI 11J01 BITS 0-3
SCM 3.3 (HT)
LQ 10I01 BITS 5,14,15
10I16 12,13
10H16 9,10,11
LQ 10H15 BITS 6,7,8
FANOUT
ADDR BITS 5-15
SCM 3,3 (BANKS 0-17)
LQ 11I01 BITS 5,14,15
11I02 12,13
11H02 9,10,11
LQ 11H01 BITS 6,7,8
SCM 3,3 (BANKS 20-37)
SL 8K08 BITS 0-3
SAS RANKS FULL XLTR
RANK A FULL: GO ADDR • NO GO • B FULL + GO ADDR • A FULL • B FULL + NO GO • A FULL
RANK B FULL: GO ADDR • NO GO • A FULL • B FULL + A FULL • B FULL + NO GO • B FULL
RANK C FULL: GO ADDR • B FULL • C FULL + B FULL • C FULL + NO GO • C FULL
SCM 3.0 (LM)
GO ADDR
SAS FLAGS XLTR
ADDR FLAG: DIV TIME 13 • (A FULL + B FULL + C FULL)
NCF: NO GO + A FULL • B FULL • C FULL
NBF: B FULL • C FULL
DIV 3.0 (DQ)
DIV TIME 13
NCF
NBF
SCM 3.0 (LM), MUX 3.4 (NM)
SCM 3.0 (LM), CPU 3.2 (LF), 3.7 (LJ)
ENTER / SELECT SAS RANKS XLTR (SAME AS SHOWN FOR SK1 AND SK2)
TAG BITS 0-3
SCM 3.0 (LM)
DESTINATION CODE TAG BITS 0-3
SCM 3,0 (9JC7)
SCM TO X TAG BITS 0-2
CPU 3.6 (RO)
STORAGE ADDRESS STACK
ADDR BITS 0-3, 4
ADDR BITS 0-4
ADDR FLAG
SM 8K12 BANKS 4-7, 10-13, 20-23, 34-37
SM 8K11 BANKS 0-3, 14-17, 24-27, 30-33
BANK SELECT XLTR
COMP
GO BANK
SCM 3.3 (BANKS 0-37)
NO GO
SCM 3.0 (9JC7)
SET BANK BUSY
BANK BUSY
SN 8K14 BANKS 20-37
SN 8K13 BANKS 0-17
BANK BUSY FLAGS REG
FREE BANK (1)
SCM 3,3 (BANKS 0-37)
MC (2)
CPU 3,2 (LI)
NOTES:
(1) FREE BANK X (1 OF 32) CLEARS BANK X BUSY FLAG.
(2) MC (MASTER CLEAR) CLEARS ALL BANK BUSY FLAGS.
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED - MODULES DIAGRAM
STORAGE ADDRESS STACK AND ADDRESS PATHS
CODE IDENT C
DWG NO 60297600
REV H
SHEET SCM 3.2
PAGE 5-225

INHIBIT REGISTERS

Each SCM Bank has a 65-bit Bank Inhibit Register (SG modules). Each SG module contains five bits of the registers for four banks. Therefore, a total of 104 modules are used for the 32 Bank Inhibit Registers.

Write Data Bits 0-59 and Parity Bits 60-64 from the SI module are present at the input of all Bank Inhibit Registers. This data is complemented and gated into the register that has a Begin Inhibit signal present from the selected bank. The Inhibit Data remains in the register until an End Inhibit signal from the selected bank is generated. This data is used by Inhibit Current Generators in the 2SB7 and 2SC7 modules during the last four clock periods of the bank read/write cycle.

MEMORY BANKS

There are 32 identical memory banks in SCM. Any one bank may begin a read/write cycle in a given clock period and complete the cycle nine clock periods later. Therefore, it is possible to have ten banks in various phases of activity during any one clock period. A functional description of an individual SCM Bank is provided for the diagram on sheet SCM 3.4.

READ DATA PATHS

READ REGISTERS AND READ DATA MERGE

There are eight Bank Read Registers (SG modules) in SCM. Each of these registers is shared by four SCM Banks. The SG modules each contain five bits of the common register for four banks. Therefore, a total of 104 modules are used for the Bank Read Registers. (These modules also contain the Bank Inhibit Registers.)

Read Data is transmitted to a Read Register from a SCM Bank during the read portion of the read/write cycle. Since only one SCM Bank may be initiated in any one clock period, there can be only one bank entering Read Data into a Read Register every clock period. The eight sets of Read Data paths from these registers are connected to a Read Data Merge network in the SH modules. This static network provides a common point for SCM Read Data from all 32 banks. The single-word output of this network is distributed to the IWS, X Register, the SRO Register, and back to the appropriate Bank Inhibit Register (thru SI modules) for memory restoration. Read Data output to an X Register is dependent on a Read SCM to X control signal from the SI module. Only the 60 data bits are sent to the IWS and X Register. The SRO and Bank Inhibit Registers also receive the five SCM parity bits.

STORAGE READ-OUT (SRO) REGISTER

The SRO Register (HP modules) is used to relay SCM Read Data to other sections of the central computer. New data enters this 65-bit register from the Read Data Merge network (SH modules) during every clock period. This register contains Read Data from the SCM Bank that has been sensed in the previous clock period. If all banks were idle, all ones enter the SRO Register. Output data from this register is sent to LCM, I/O Multiplexer, or exchange package registers. The data is gated at the receiving end of these transmission paths. However, data sent to the A and B Registers during an exchange sequence is dependent on a Gate Exchange Data signal from the HU module. Data sent to the I/O Multiplexer is first entered into an I/O Output Buffer Register (HM modules).

PARITY CHECK

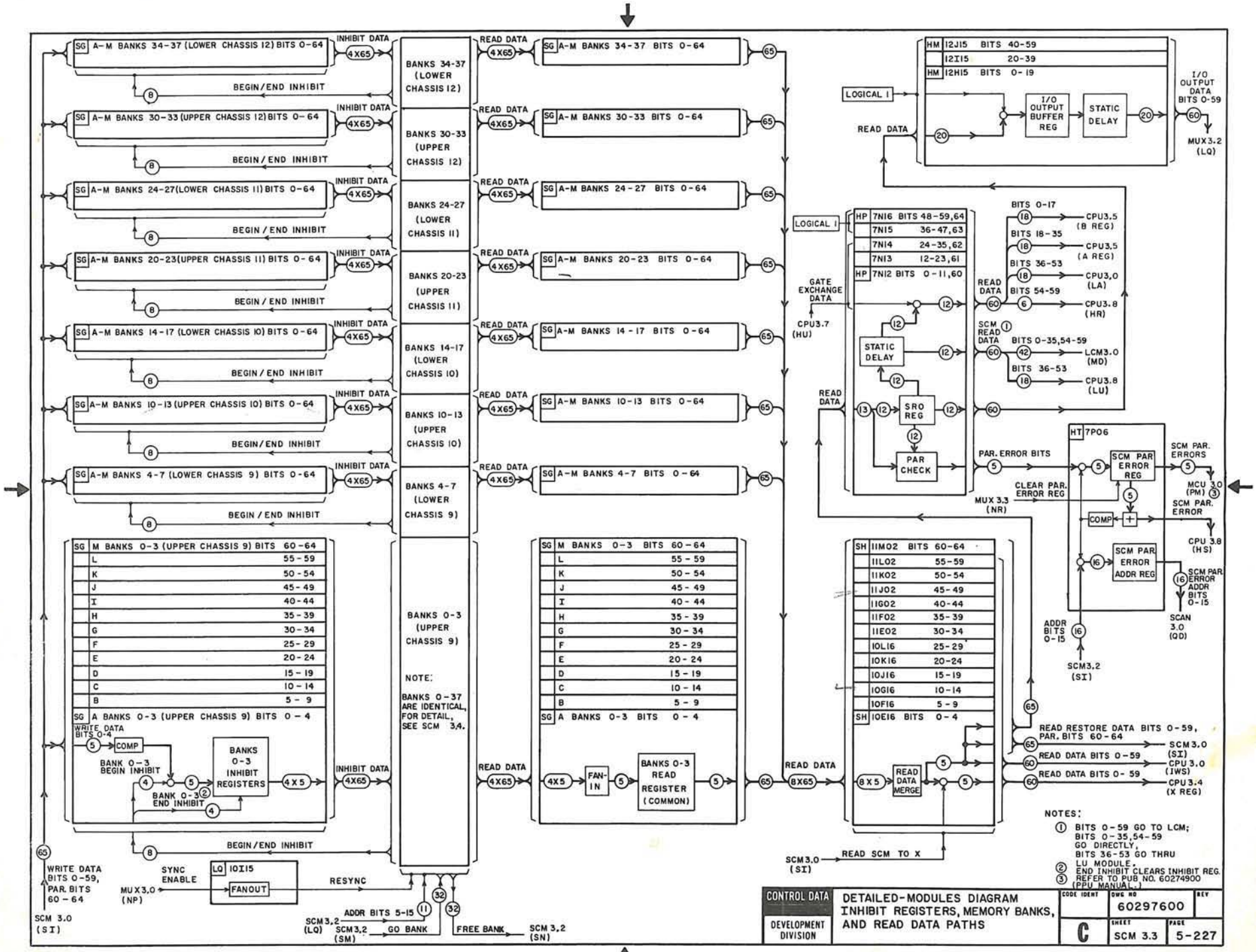
The data in the SRO Register is merged in a Parity Check network (HP modules). This network checks the 13 bits in each of the five fields of the 65-bit word. Each field corresponds to 13 bits in an SCM storage module (9SA7 module). If no parity errors exist, each field will contain an odd number of one bits and the Parity Check network will output five zero Parity Error Bits. If a parity error has occurred, the corresponding field will contain an even number of one bits and the Parity Check network will output a one and four zero Parity Error Bits.

SCM PARITY ERROR REGISTER

The output of the Parity Check network is sent to the SCM Parity Error Register (HT module). Any previous error data must be cleared before new data can be entered. This register is monitored by the MCU (PM module) for SCM Parity Errors. The PSD register (HS module) is also informed if a SCM Parity Error has occurred.

SCM PARITY ERROR ADDRESS REGISTER

The error address is held in the SCM Parity Error Address Register (HT module). This register is monitored by the MCU Scanner (QD modules). SCM addresses are entered into this register every clock period if none of the SCM Parity Error Register bits are ones. When a parity error does occur, one or more of these bits will be a one. This blocks entry of any subsequent addresses in the SCM Parity Error Address Register. The SCM address at which the parity error occurred is held in the register.


SG A-M BANKS 34-37 (LOWER CHASSIS 12) BITS 0-64
SG A-M BANKS 30-33 (UPPER CHASSIS 12) BITS 0-64
SG A-M BANKS 24-27 (LOWER CHASSIS 11) BITS 0-64
SG A-M BANKS 20-23 (UPPER CHASSIS 11) BITS 0-64
SG A-M BANKS 14-17 (LOWER CHASSIS 10) BITS 0-64
SG A-M BANKS 10-13 (UPPER CHASSIS 10) BITS 0-64
SG A-M BANKS 4-7 (LOWER CHASSIS 9) BITS 0-64
INHIBIT DATA
4X65
BEGIN/END INHIBIT
BANKS 34-37 (LOWER CHASSIS 12)
BANKS 30-33 (UPPER CHASSIS 12)
BANKS 24-27 (LOWER CHASSIS 11)
BANKS 20-23 (UPPER CHASSIS 11)
BANKS 14-17 (LOWER CHASSIS 10)
BANKS 10-13 (UPPER CHASSIS 10)
BANKS 4-7 (LOWER CHASSIS 9)
SG M BANKS 0-3 (UPPER CHASSIS 9) BITS 60-64
L 55-59
K 50-54
J 45-49
I 40-44
H 35-39
G 30-34
F 25-29
E 20-24
D 15-19
C 10-14
B 5-9
SG A BANKS 0-3 (UPPER CHASSIS 9) BITS 0-4
WRITE DATA BITS 0-4
COMP
BANK 0-3 BEGIN INHIBIT
BANK 0-3 END INHIBIT
BANKS 0-3 INHIBIT REGISTERS
4X5
BANKS 0-3 (UPPER CHASSIS 9)
NOTE:
BANKS 0-37 ARE IDENTICAL, FOR DETAIL, SEE SCM 3.4.
WRITE DATA BITS 0-59, PAR. BITS 60-64
SCM 3.0 (SI)
SYNC ENABLE
MUX 3.0 (NP)
LQ 10I15
FANOUT
RESYNC
ADDR BITS 5-15
SCM 3.2 (LQ)
SCM 3.2 (SM)
GO BANK
FREE BANK
SCM 3.2 (SN)
READ DATA
4X65
SG A-M BANKS 34-37 BITS 0-64
SG A-M BANKS 30-33 BITS 0-64
SG A-M BANKS 24-27 BITS 0-64
SG A-M BANKS 20-23 BITS 0-64
SG A-M BANKS 14-17 BITS 0-64
SG A-M BANKS 10-13 BITS 0-64
SG A-M BANKS 4-7 BITS 0-64
SG M BANKS 0-3 BITS 60-64
L 55-59
K 50-54
J 45-49
I 40-44
H 35-39
G 30-34
F 25-29
E 20-24
D 15-19
C 10-14
B 5-9
SG A BANKS 0-3 BITS 0-4
4X5
FAN-IN
BANKS 0-3 READ REGISTER (COMMON)
8X65
8X5
READ DATA MERGE
HM 12J15 BITS 40-59
12I15 20-39
HM 12H15 BITS 0-19
LOGICAL 1
I/O OUTPUT BUFFER REG
STATIC DELAY
I/O OUTPUT DATA BITS 0-59
MUX 3.2 (LQ)
HP 7N16 BITS 48-59,64
7N15 36-47,63
7N14 24-35,62
7N13 12-23,61
HP 7N12 BITS 0-11,60
GATE EXCHANGE DATA
CPU 3.7 (HU)
STATIC DELAY
SRO REG
PAR CHECK
BITS 0-17
CPU 3.5 (B REG)
BITS 18-35
CPU 3.5 (A REG)
BITS 36-53
CPU 3.0 (LA)
BITS 54-59
CPU 3.8 (HR)
SCM READ DATA
BITS 0-35,54-59
LCM 3.0 (MD)
BITS 36-53
CPU 3.8 (LU)
PAR. ERROR BITS
CLEAR PAR. ERROR REG
MUX 3.3 (NR)
HT 7P06
SCM PAR ERROR REG
SCM PAR. ERRORS
MCU 3.0 (PM)
COMP
SCM PAR. ERROR
CPU 3.8 (HS)
SCM PAR ERROR ADDR REG
SCM PAR ERROR ADDR BITS 0-15
SCAN 3.0 (QD)
ADDR BITS 0-15
SCM 3.2 (SI)
SH 11M02 BITS 60-64
11L02 55-59
11K02 50-54
11J02 45-49
11G02 40-44
11F02 35-39
11E02 30-34
10L16 25-29
10K16 20-24
10J16 15-19
10G16 10-14
10F16 5-9
SH 10E16 BITS 0-4
READ RESTORE DATA BITS 0-59, PAR. BITS 60-64
SCM 3.0 (SI)
READ DATA BITS 0-59
CPU 3.0 (IWS)
READ DATA BITS 0-59
CPU 3.4 (X REG)
SCM 3.0 (SI)
READ SCM TO X
NOTES:
① BITS 0-59 GO TO LCM; BITS 0-35,54-59 GO DIRECTLY, BITS 36-53 GO THRU LU MODULE.
② END INHIBIT CLEARS INHIBIT REG.
③ REFER TO PUB NO. 60274900 (PPU MANUAL.)
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM
INHIBIT REGISTERS, MEMORY BANKS, AND READ DATA PATHS
CODE IDENT
C
DWG NO
60297600
REV
SHEET
SCM 3.3
PAGE
5-227

DETAILED-MODULES DIAGRAM
SCM BANK (1 OF 32 IDENTICAL BANKS)

Each SCM Bank contains ten 9SA7 modules, ten 2SB7 modules, ten 2SC7 modules, two SD modules, one SE module, and one SF module. The 9SA7 modules each contain a core memory stack of 32 x 32 x 13 cores plus the horizontal and vertical read/write drive circuits. All 65-bit (including parity) words with address bit 5 equal to zero are stored in five even stacks. All words with address bit 5 equal to one are stored in five odd stacks. The 2SB7 and 2SC7 modules are similar to each other in that each contains part of the inhibit and sense circuits. Each 2SB7 module contains seven inhibit drives and six sense amplifiers. Each 2SC7 module contains six inhibit drives and seven sense amplifiers. The SD modules contain the Bank Address Register. This register contains address bits 6-15 which are fanned-out to each 9SA7 module. The SE module contains the Bank Sequence Control. This module controls bank activity during the read/write cycle. The SF module contains a fanout for address bits 5, 10, and 15 to the 2SB7 and 2SC7 modules and Begin/End Inhibit signals to the Bank Inhibit Registers (SG modules).

READ/WRITE CYCLE INITIATION

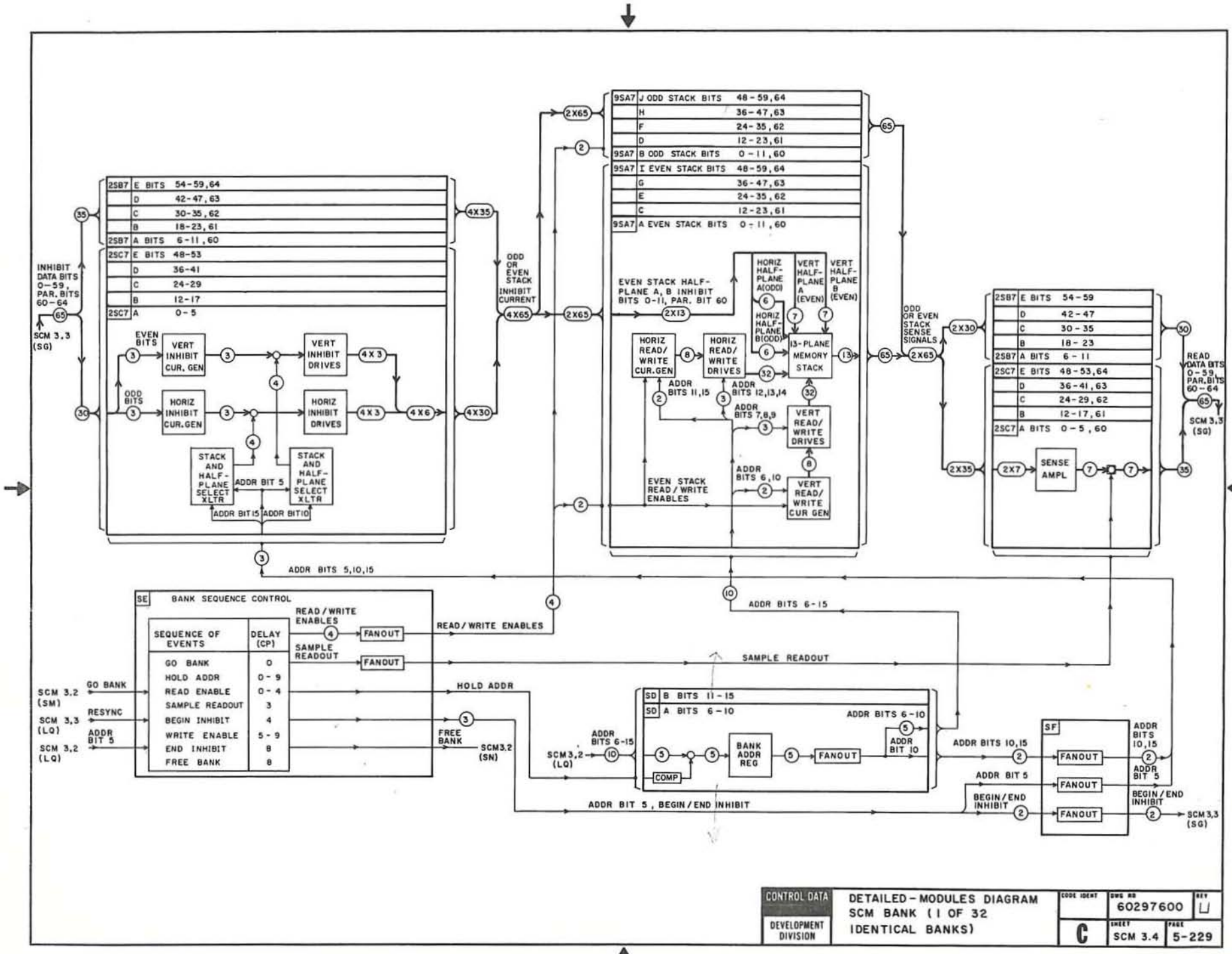
A bank read/write cycle begins when a Go Bank signal has been generated by the SM module. At this time, Address Bits 6-15 are entered into the Bank Address Register (SD modules) from the SAS. This address is held in the register until the cycle is complete.

READ/SENSE

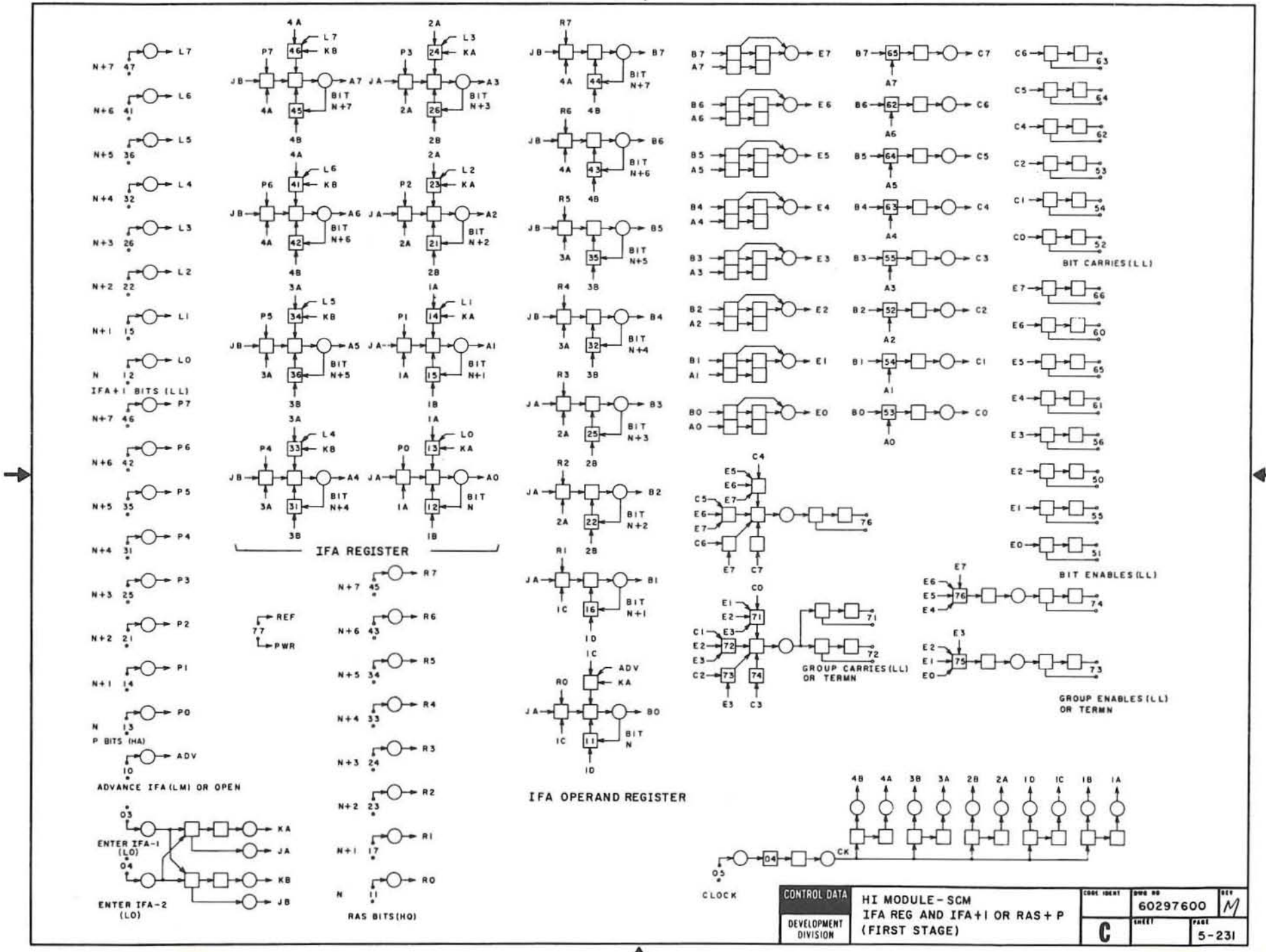
The read portion of the bank read/write cycle begins when the Bank Sequence Control generates a Read Enable signal. Bits 6-10 of the address select the vertical drive and bits 11-15 select the horizontal drive on the 9SA7 modules. During the read cycle, current flows thru the selected drive lines and Sense Signals from the selected cores are generated. These signals are amplified by the 2SB7 and 2SC7 modules and gated to a Bank Read Register which is shared with three other banks. Since a read cycle destroys the selected word in memory, a write or restoration cycle follows.

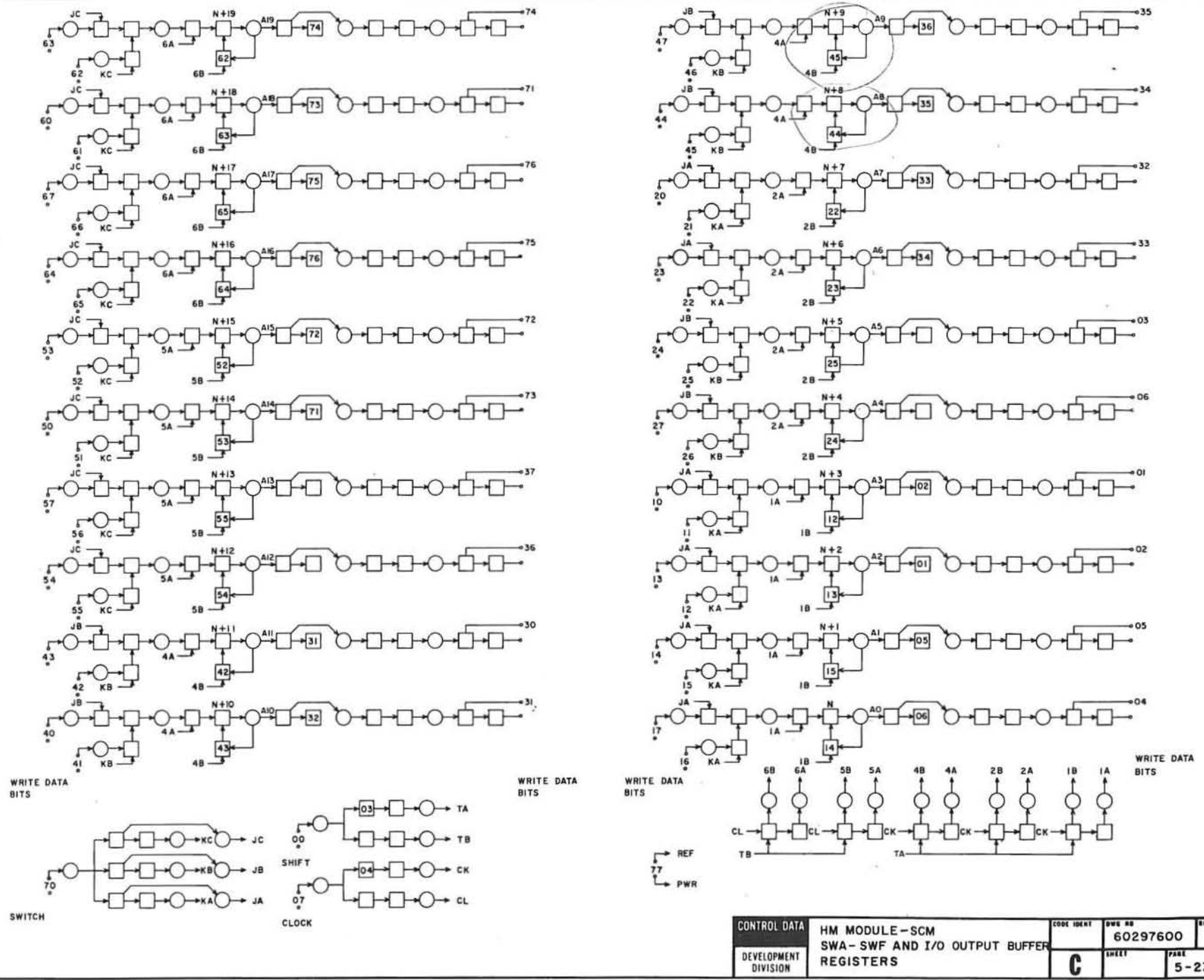
WRITE/INHIBIT

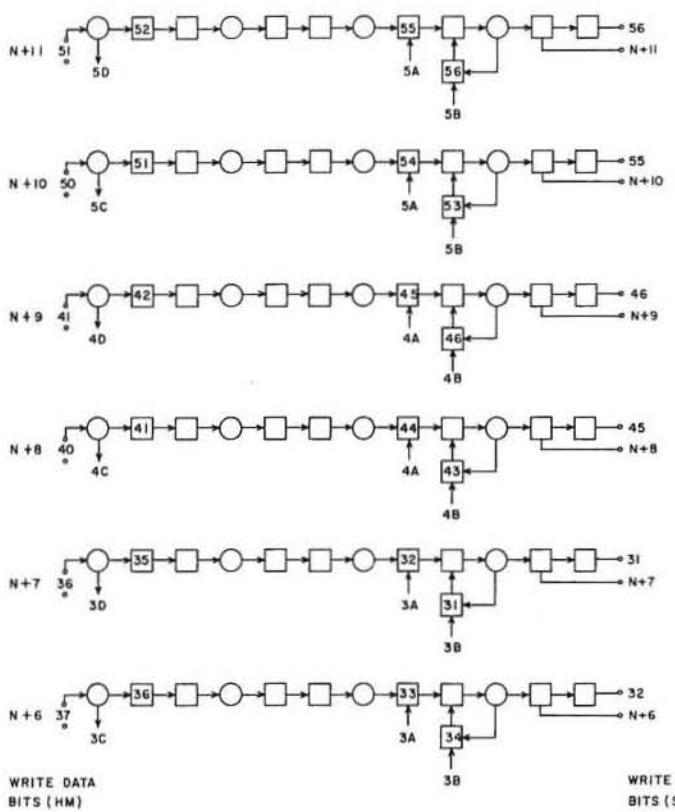
The write portion of the bank read/write cycle begins when Begin Inhibit and Write Enable signals are generated by the Bank Sequence Control. Current flows thru the previously selected drive lines in the opposite direction than during the read cycle. Since unopposed write current would switch all selected cores to a one state, an inhibit current is generated when a zero state is desired. The inhibit current flows through inhibit lines which are arranged in two parallel groups of 16 lines each on each memory plane. They are vertically oriented on the even planes and horizontally oriented on the odd planes. Inhibit current is generated for the selected word by the bits that are set in the Bank Inhibit Registers (one for each bank) in the SG modules. These registers hold the complement of write data. The inhibit current is directed to the correct stack and half-plane by a translation and distribution network in the 2SB7 and 2SC7 modules. Bit 5 of the address selects the stack; bit 10, the most significant of the vertical select bits, selects the vertical half-planes; bit 15, the most significant of the horizontal select bits, selects the horizontal half-planes.

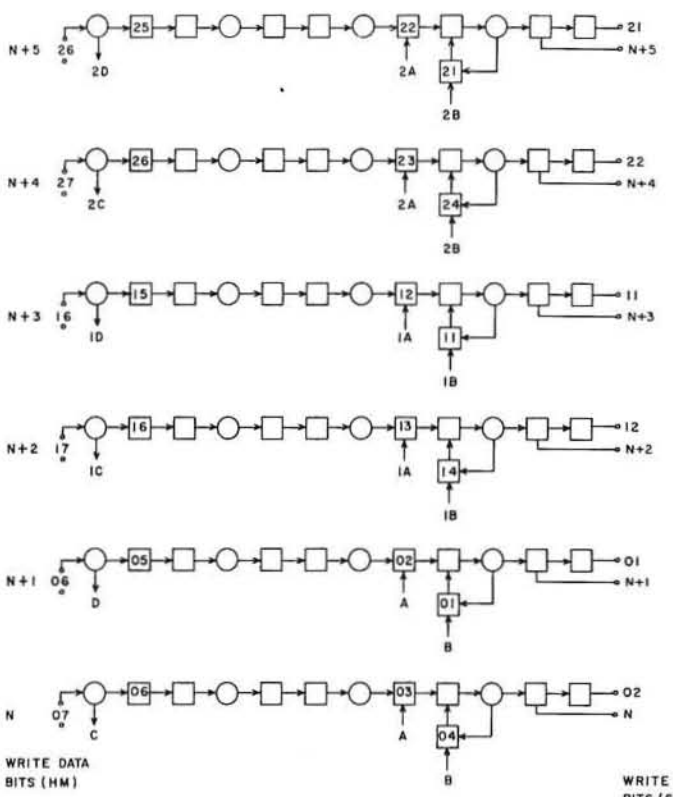


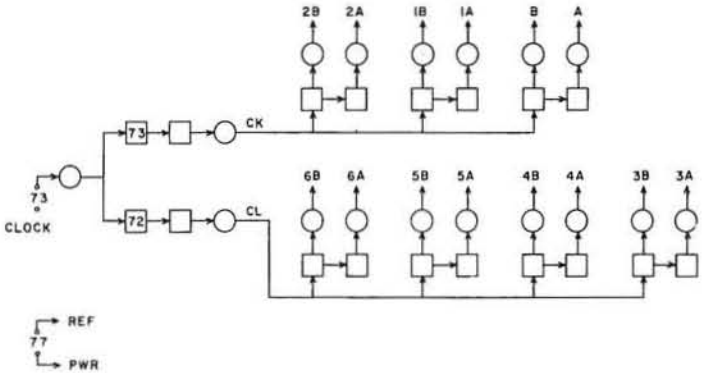
CONTROL DATA	DETAILED - MODULES DIAGRAM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	SCM BANK (1 OF 32 IDENTICAL BANKS)	C	60297600	U
		SHEET SCM 3.4	PAGE 5-229	

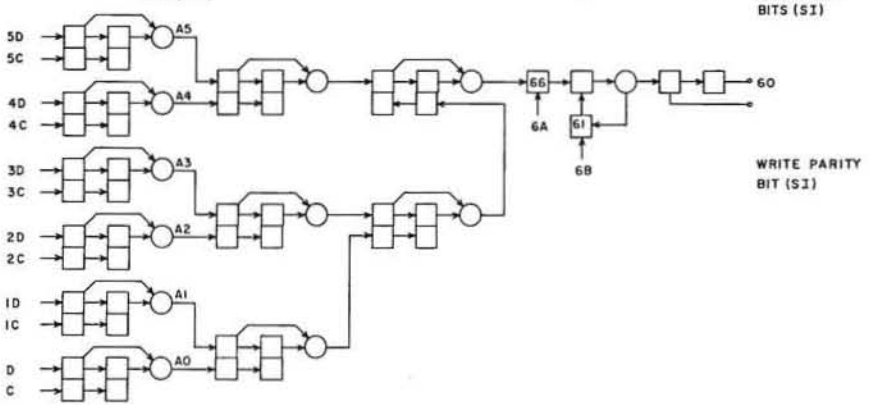

IFA REGISTER
IFA OPERAND REGISTER
IFA+1 BITS (LL)
P BITS (HA)
ADVANCE IFA (LM) OR OPEN
ENTER IFA-1 (LO)
ENTER IFA-2 (LO)
RAS BITS (HQ)
BIT CARRIES (LL)
BIT ENABLES (LL)
GROUP CARRIES (LL) OR TERMN
GROUP ENABLES (LL) OR TERMN
CLOCK
REF
PWR
ADV
BIT N+7
BIT N+6
BIT N+5
BIT N+4
BIT N+3
BIT N+2
BIT N+1
BIT N
CONTROL DATA
DEVELOPMENT DIVISION
HI MODULE - SCM
IFA REG AND IFA+1 OR RAS + P
(FIRST STAGE)
60297600
C
5-231


WRITE DATA BITS
WRITE DATA BITS
WRITE DATA BITS
WRITE DATA BITS
SWITCH
CLOCK
SHIFT
REF
PWR
CONTROL DATA
DEVELOPMENT DIVISION
HM MODULE-SCM
SWA-SWF AND I/O OUTPUT BUFFER REGISTERS
60297600
C
5-233

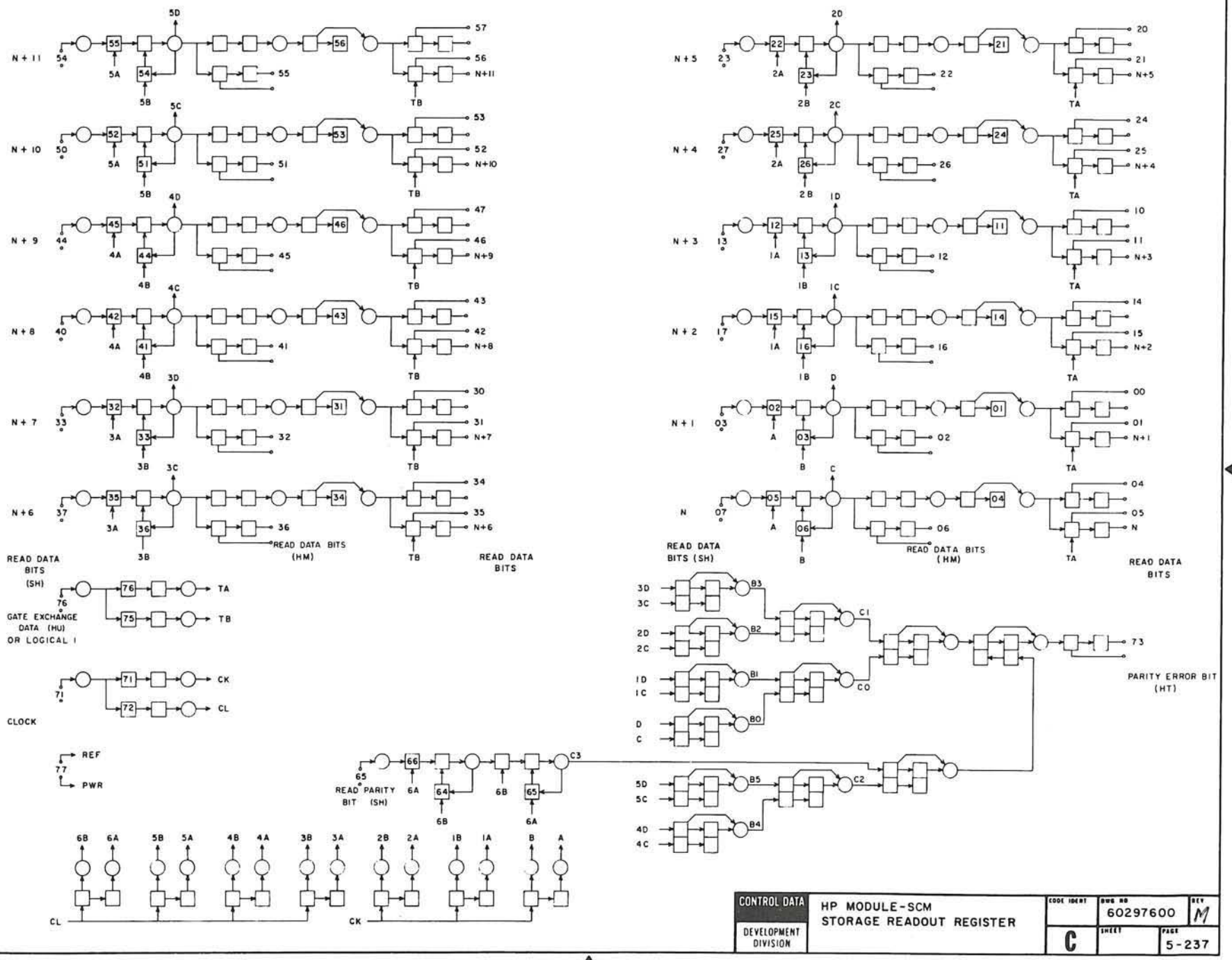






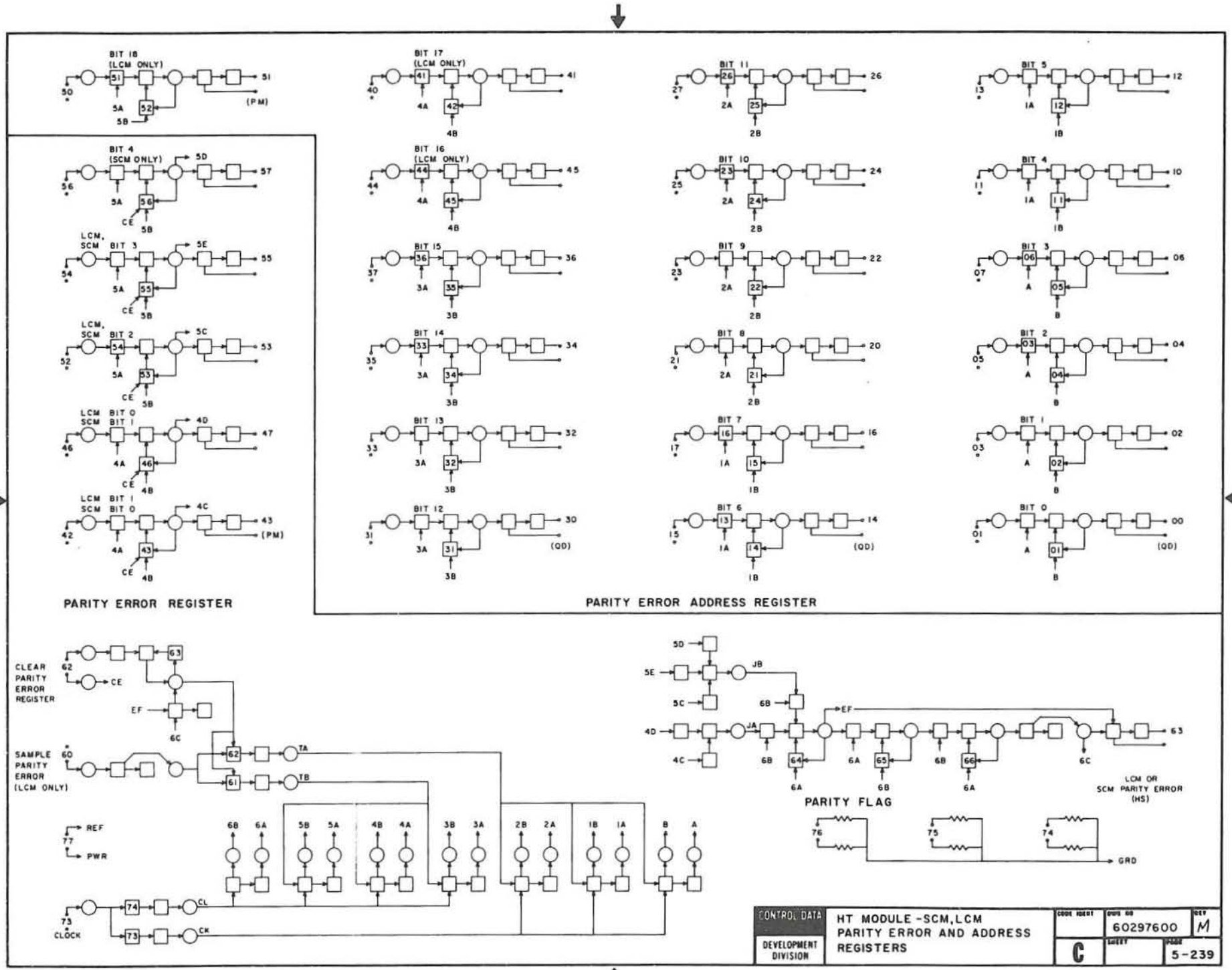


CONTROL DATA DEVELOPMENT DIVISION	HN MODULE - SCM SWG REGISTER AND PARITY GENERATOR	CODE IDENT C	DWG NO 60297600	REV
			SHEET	PAGE 5-235

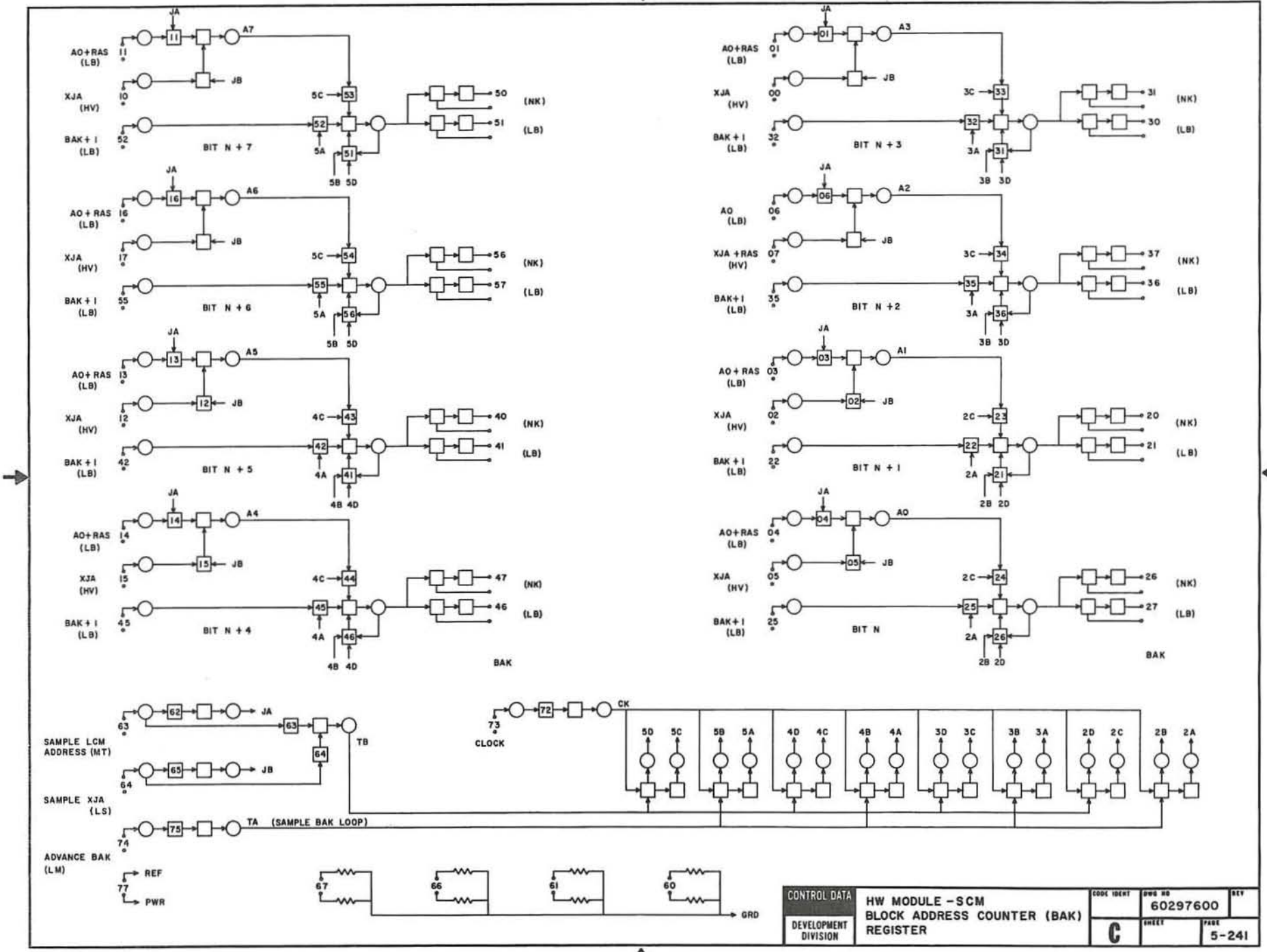

N + 11
N + 10
N + 9
N + 8
N + 7
N + 6
N + 5
N + 4
N + 3
N + 2
N + 1
N
READ DATA BITS (SH)
READ DATA BITS (HM)
READ DATA BITS
GATE EXCHANGE DATA (HU) OR LOGICAL 1
CLOCK
REF
PWR
READ PARITY BIT (SH)
PARITY ERROR BIT (HT)
CONTROL DATA
DEVELOPMENT DIVISION
HP MODULE-SCM
STORAGE READOUT REGISTER
CODE IDENT
C
DWG NO
60297600
REV
M
SHEET
PAGE
5-237

The HT module contains a five-bit SCM Parity Error Register and a 16-bit SCM Parity Error Address Register. Both registers are normally cleared and entered with new information every clock period under gated clock pulse control. This occurs when no parity errors exist in the word read from SCM. When no errors exist, the Parity Flag will be clear and the bit holding register (test point 63) will be set. The AND gates will be made (TA and TB terms present) at this time to enable the clock pulses. (The second input to the gates are constant ones since the Sample Parity Error input is open.)

If any of the SCM Parity Error Register bits are set during a given clock period, the Parity Flag will set. This clears the bit holding register (test point 63) since both EF and 6C terms will be present for one clock period. Therefore, the AND gates will be broken (TA and TB terms absent) and the clock pulses will be disabled. At this time, the SCM Parity Error Address Register will contain the address in SCM at which an error has occurred. Also, the Parity Error Register will indicate which section of the 60-bit word has been misread from memory. Normal operation will be restored when the Clear Parity Error Register signal is applied.

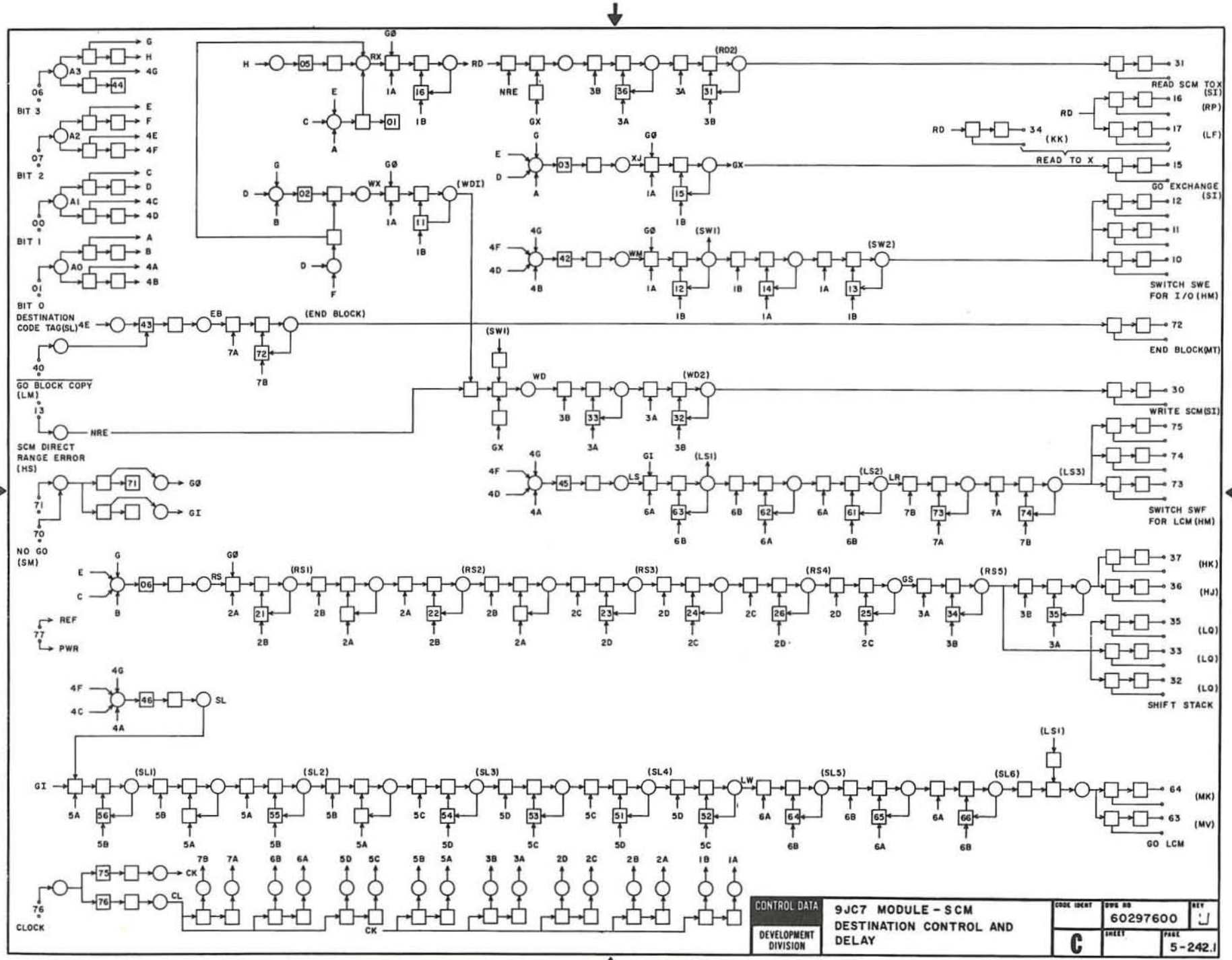


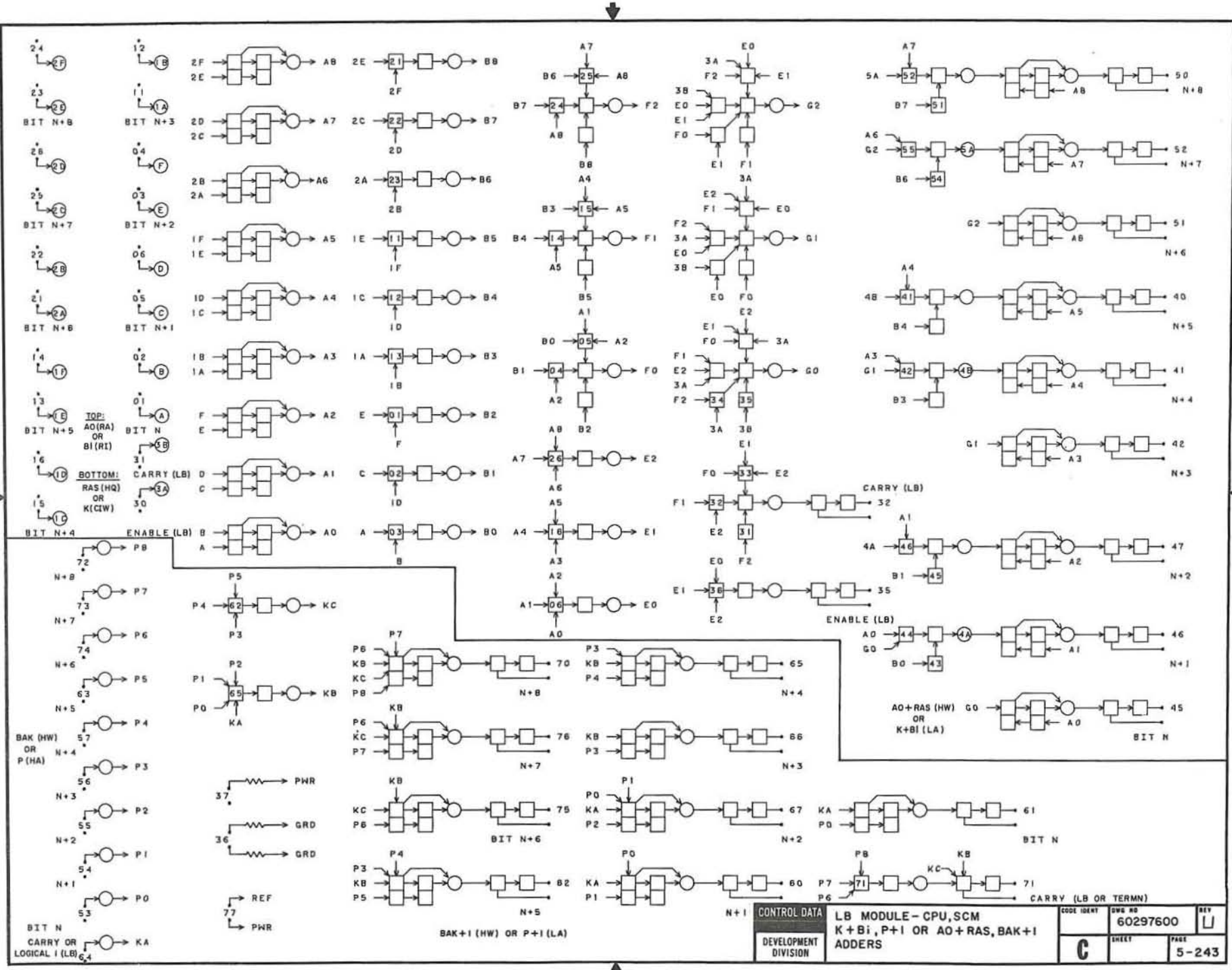
CONTROL DATA DEVELOPMENT DIVISION	HT MODULE - SCM, LCM PARITY ERROR AND ADDRESS REGISTERS	CODE IDENT C	DWG NO 60297600	REV M
			SHEET	PAGE 5-239


BIT N + 7
BIT N + 6
BIT N + 5
BIT N + 4
BIT N + 3
BIT N + 2
BIT N + 1
BIT N
BAK
AO+RAS (LB)
XJA (HV)
BAK + 1 (LB)
AO (LB)
XJA +RAS (HV)
JA
JB
(NK)
(LB)
SAMPLE LCM ADDRESS (MT)
SAMPLE XJA (LS)
ADVANCE BAK (LM)
REF
PWR
CLOCK
CK
TA (SAMPLE BAK LOOP)
TB
GRD
CONTROL DATA
DEVELOPMENT DIVISION
HW MODULE - SCM
BLOCK ADDRESS COUNTER (BAK) REGISTER
CODE IDENT
C
DWG NO
60297600
REV
SHEET
PAGE
5-241

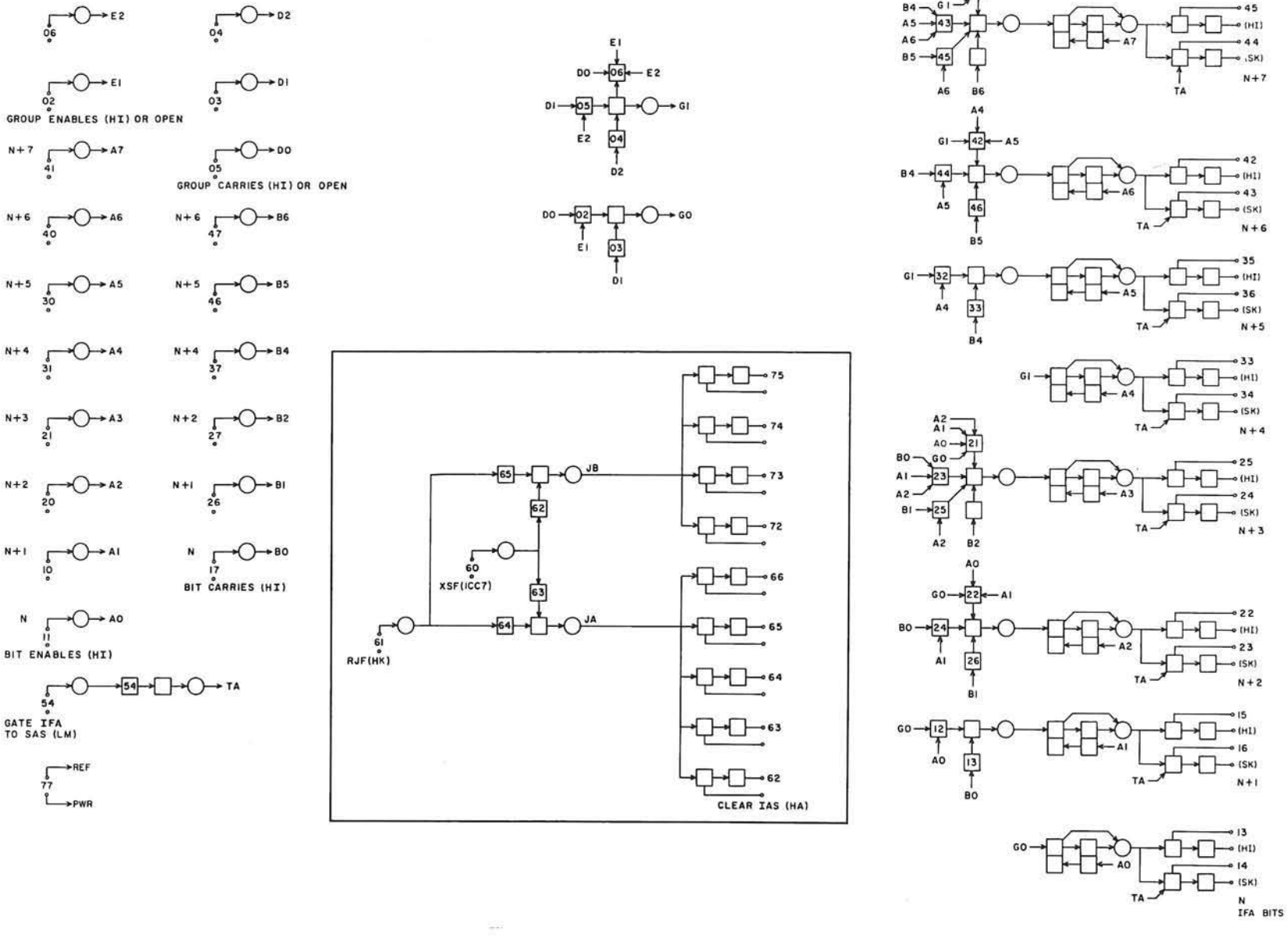
9JC7 MODULE

The 9JC7 module translates Destination Code Tag Bits 0-3 which are received from the SAS (SL module) during each clock period. As a result of this translation, one or more control signals are sent to the SCM, LCM, or CPU. These signals are delayed by timing chains of various lengths. The AND gates preceding the first FF of the timing chains are enabled by the Destination Code Tag Bits. For example, the shift stack timing chain (RS1-RS5 terms) is enabled when these bits equal 0001.

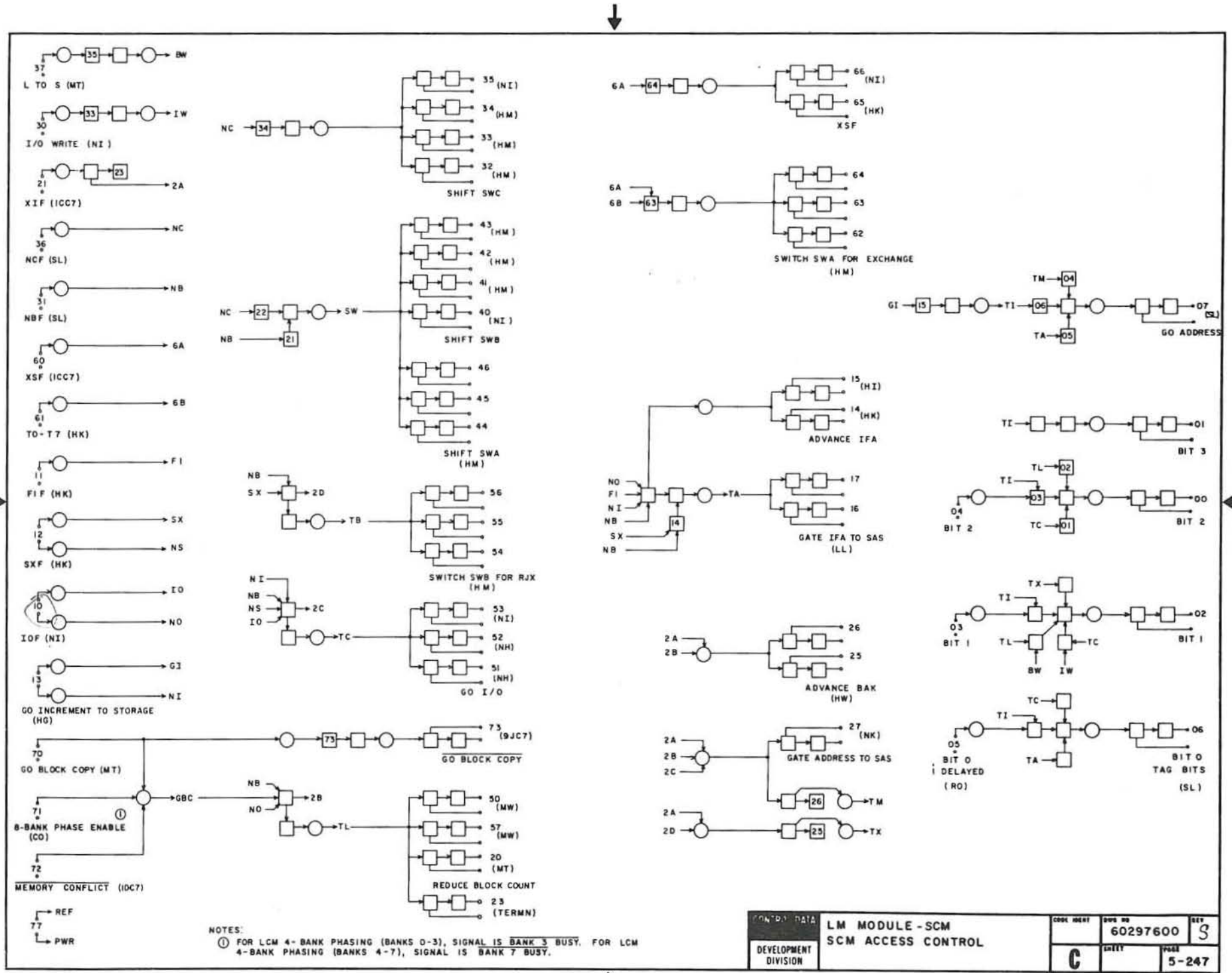

BIT 3
BIT 2
BIT 1
BIT 0
DESTINATION CODE TAG(SL)
GO BLOCK COPY (LM)
SCM DIRECT RANGE ERROR (HS)
NO GO (SM)
CLOCK
(END BLOCK)
READ SCM TO X
READ TO X
GO EXCHANGE (SI)
SWITCH SWE FOR I/O (HM)
END BLOCK(MT)
WRITE SCM(SI)
SWITCH SWF FOR LCM (HM)
SHIFT STACK
GO LCM
CONTROL DATA
DEVELOPMENT DIVISION
9JC7 MODULE - SCM
DESTINATION CONTROL AND
DELAY
CODE IDENT
C
DWG NO
60297600
REV
J
SHEET
PAGE
5-242.1

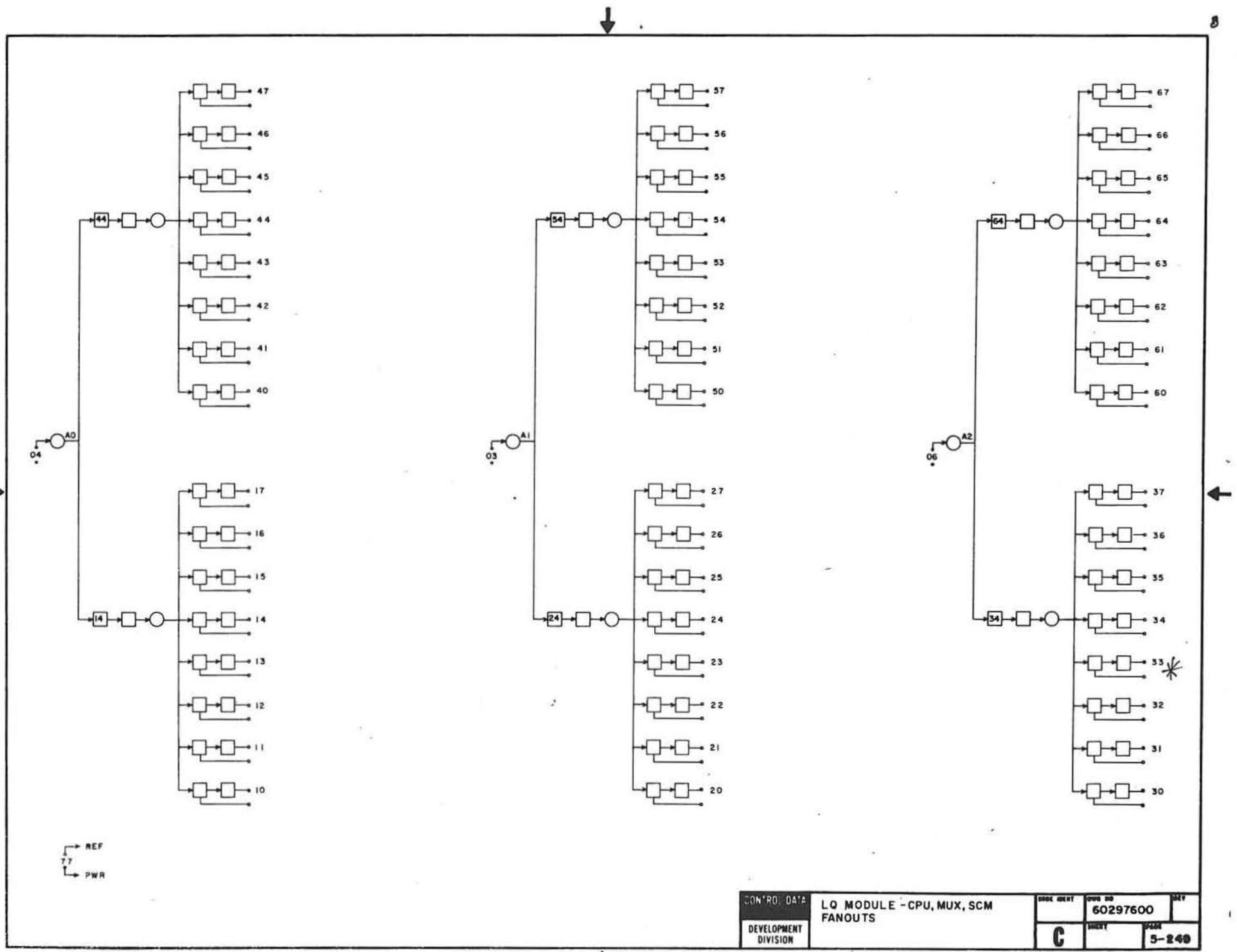


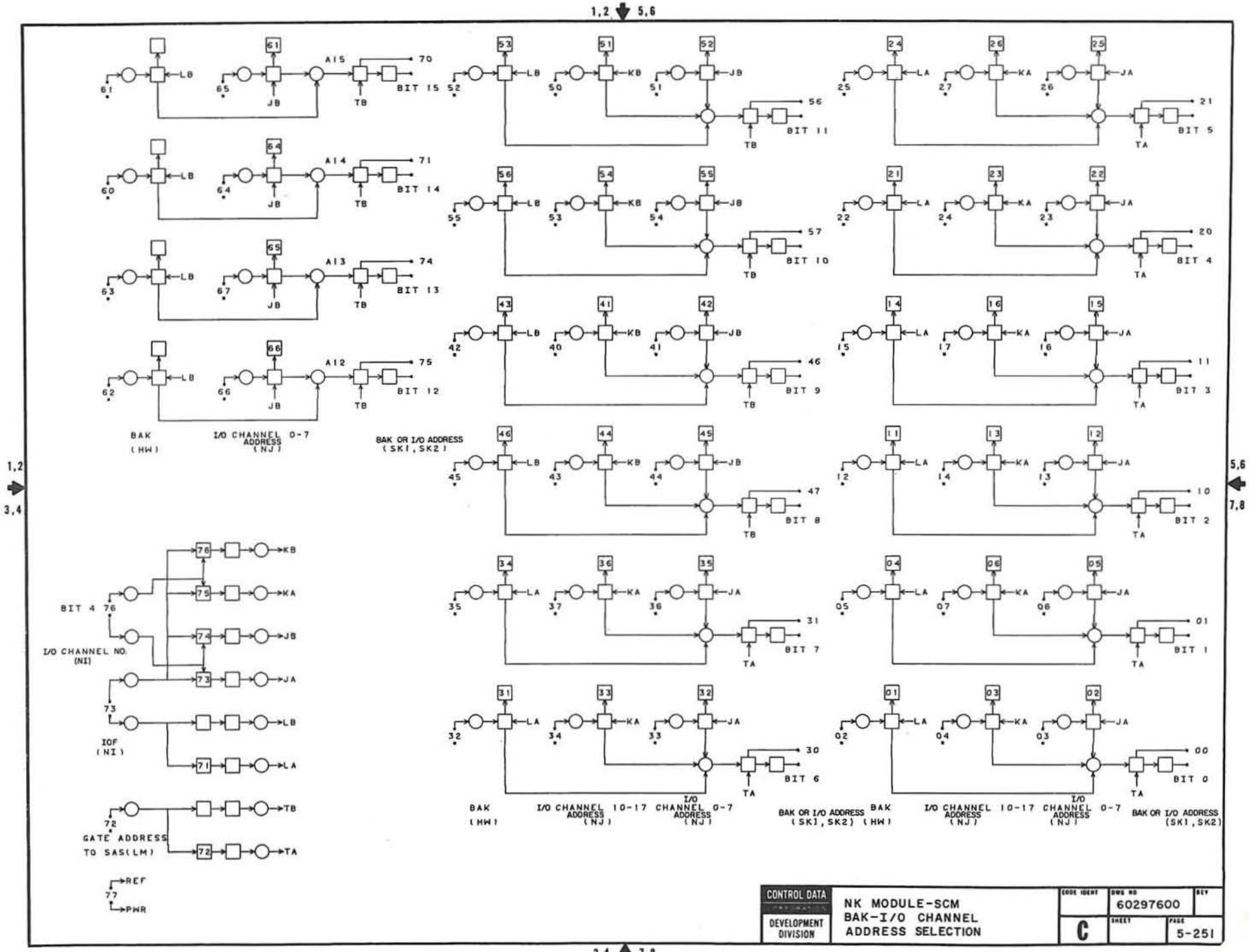
CONTROL DATA	LB MODULE - CPU, SCM K+Bi, P+1 OR AO+RAS, BAK+1 ADDERS	CODE IDENT	DWG NO 60297600	REV U
DEVELOPMENT DIVISION		C	SHEET	PAGE 5-243



CONTROL DATA	LL MODULE - SCM, CPU IFA+1 OR RAS+P (SECOND STAGE); CLR IAS FANOUT	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	
		SHEET	PAGE	5-245


L TO S (MT)
I/O WRITE (NI)
XIF (ICC7)
NCF (SL)
NBF (SL)
XSF (ICC7)
TO-T7 (HK)
FIF (HK)
SXF (HK)
IOF (NI)
GO INCREMENT TO STORAGE (HG)
GO BLOCK COPY (MT)
8-BANK PHASE ENABLE (CO)
MEMORY CONFLICT (IDC7)
SHIFT SWC
SHIFT SWB
SHIFT SWA (HM)
SWITCH SWB FOR RJX (HM)
GO I/O
REDUCE BLOCK COUNT
GO BLOCK COPY
XSF
SWITCH SWA FOR EXCHANGE (HM)
ADVANCE IFA
GATE IFA TO SAS (LL)
ADVANCE BAK (HW)
GATE ADDRESS TO SAS
GO ADDRESS
BIT 3
BIT 2
BIT 1
BIT 0 TAG BITS (SL)
BIT 0 DELAYED (RO)
NOTES:
① FOR LCM 4-BANK PHASING (BANKS 0-3), SIGNAL IS BANK 3 BUSY. FOR LCM 4-BANK PHASING (BANKS 4-7), SIGNAL IS BANK 7 BUSY.
CONTROL DATA
DEVELOPMENT DIVISION
LM MODULE - SCM
SCM ACCESS CONTROL
CODE IDENT C
DWG NO 60297600
REV S
SHEET
PAGE 5-247

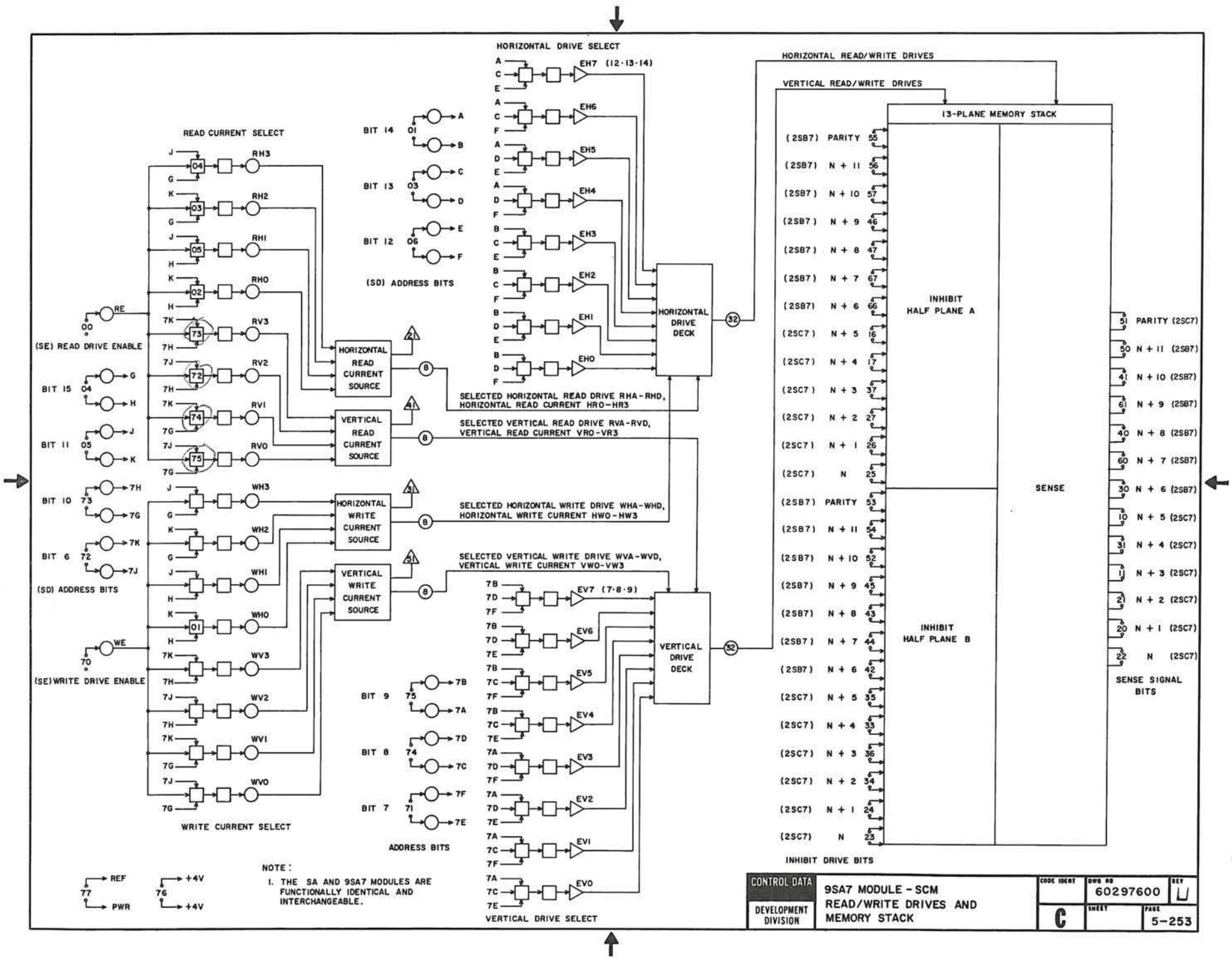

47
46
45
44
43
42
41
40
44
A0
04
17
16
15
14
13
12
11
10
14
57
56
55
54
53
52
51
50
54
A1
03
27
26
25
24
23
22
21
20
24
67
66
65
64
63
62
61
60
64
A2
06
37
36
35
34
33
32
31
30
34
REF
7.7
PWR
CONTROL DATA
DEVELOPMENT DIVISION
LQ MODULE - CPU, MUX, SCM FANOUTS
C
60297600
5-249


1,2 5,6
3,4 7,8
BAK (HW)
I/O CHANNEL 0-7 ADDRESS (NJ)
BAK OR I/O ADDRESS (SK1, SK2)
I/O CHANNEL 10-17 ADDRESS (NJ)
I/O CHANNEL 0-7 ADDRESS (NJ)
BIT 4
I/O CHANNEL NO. (NI)
IOF (NI)
GATE ADDRESS TO SAS(LM)
REF
PWR
CONTROL DATA
DEVELOPMENT DIVISION
NK MODULE-SCM
BAK-I/O CHANNEL
ADDRESS SELECTION
CODE IDENT
C
DWG NO
60297600
REV
SHEET
PAGE
5-251

9SA7 MODULE

The 9SA7 module contains a coincident current memory stack of 1024 13-bit (including a parity bit) words and the associated read and write drive circuits.

The stack consists of 13 core-array planes each having 1024 cores in a 32 by 32 configuration. Each plane has 32 vertical drive wires, 32 horizontal drive wires, one sense winding, and two inhibit windings. Each inhibit winding links 512 cores on one-half of the plane. On even planes, the inhibit wire is parallel to the vertical drive wire. On odd planes, the inhibit wire is parallel to the horizontal drive wire. Selection of one of the 32 read or write drives is determined by Bank Address Bits 11 through 15 (horizontal drives) and 6 through 10 (vertical drives). A Read Drive Enable input to the module results in current flow through the selected horizontal and vertical drive lines. A Write Drive Enable input results in current flow in the opposite direction through the drive lines.

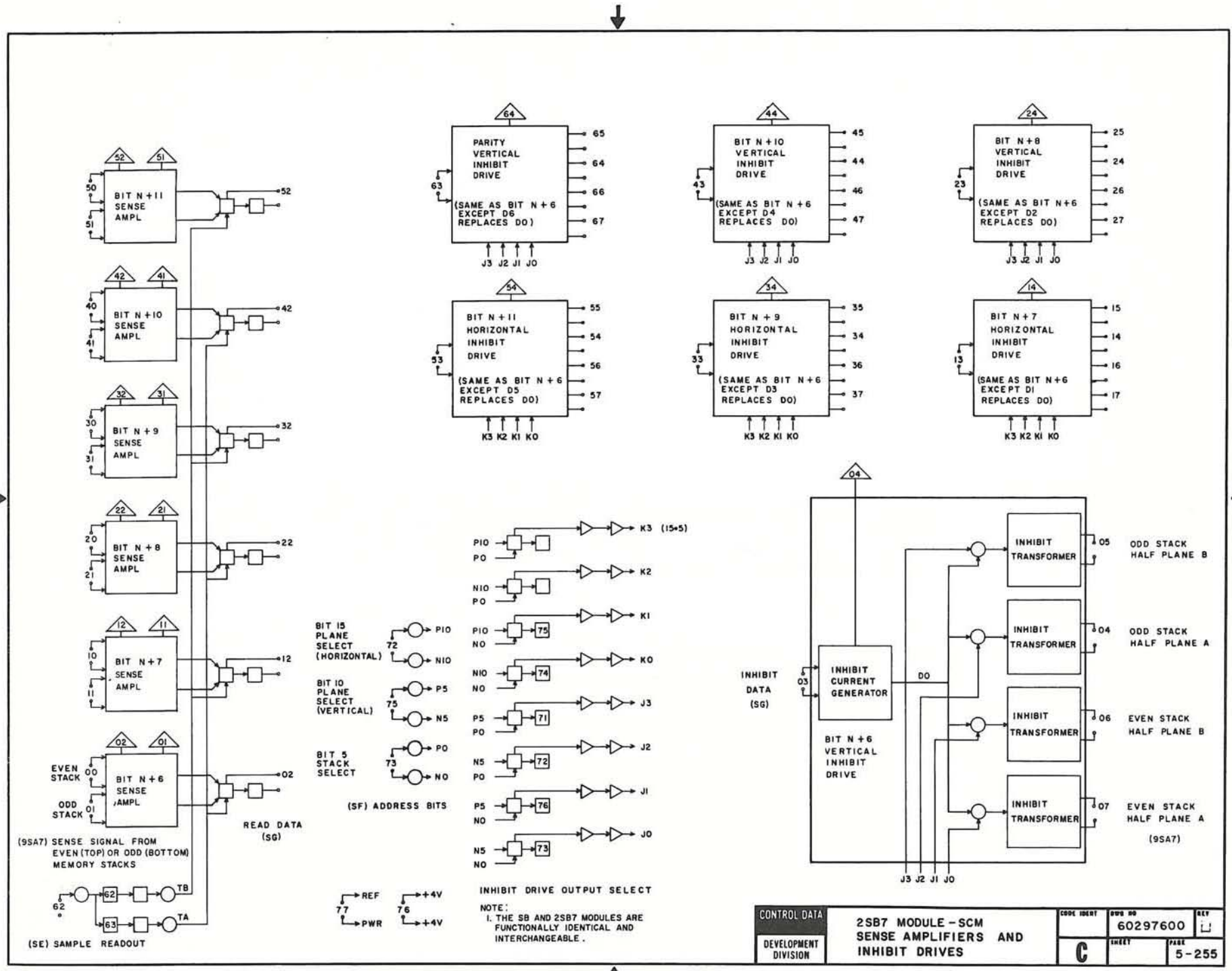

HORIZONTAL DRIVE SELECT
HORIZONTAL READ/WRITE DRIVES
VERTICAL READ/WRITE DRIVES
13-PLANE MEMORY STACK
READ CURRENT SELECT
BIT 14
BIT 13
BIT 12
(SD) ADDRESS BITS
RH3
RH2
RH1
RH0
RV3
RV2
RV1
RV0
RE
(SE) READ DRIVE ENABLE
BIT 15
BIT 11
HORIZONTAL READ CURRENT SOURCE
VERTICAL READ CURRENT SOURCE
EH7 (12-13-14)
EH6
EH5
EH4
EH3
EH2
EH1
EH0
HORIZONTAL DRIVE DECK
SELECTED HORIZONTAL READ DRIVE RHA-RHD, HORIZONTAL READ CURRENT HR0-HR3
SELECTED VERTICAL READ DRIVE RVA-RVD, VERTICAL READ CURRENT VR0-VR3
(2SB7) PARITY 55
(2SB7) N + 11 56
(2SB7) N + 10 57
(2SB7) N + 9 46
(2SB7) N + 8 47
(2SB7) N + 7 67
(2SB7) N + 6 66
(2SC7) N + 5 16
(2SC7) N + 4 17
(2SC7) N + 3 37
(2SC7) N + 2 27
(2SC7) N + 1 26
(2SC7) N 25
(2SB7) PARITY 53
(2SB7) N + 11 54
(2SB7) N + 10 52
(2SB7) N + 9 45
(2SB7) N + 8 43
(2SB7) N + 7 44
(2SB7) N + 6 42
(2SC7) N + 5 35
(2SC7) N + 4 33
(2SC7) N + 3 36
(2SC7) N + 2 34
(2SC7) N + 1 24
(2SC7) N 23
INHIBIT DRIVE BITS
INHIBIT HALF PLANE A
INHIBIT HALF PLANE B
SENSE
51 PARITY (2SC7)
50 N + 11 (2SB7)
41 N + 10 (2SB7)
61 N + 9 (2SB7)
40 N + 8 (2SB7)
60 N + 7 (2SB7)
30 N + 6 (2SB7)
10 N + 5 (2SC7)
31 N + 4 (2SC7)
11 N + 3 (2SC7)
21 N + 2 (2SC7)
20 N + 1 (2SC7)
22 N (2SC7)
SENSE SIGNAL BITS
WRITE CURRENT SELECT
BIT 10
BIT 6
(SD) ADDRESS BITS
WH3
WH2
WH1
WH0
WV3
WV2
WV1
WV0
WE
(SE) WRITE DRIVE ENABLE
HORIZONTAL WRITE CURRENT SOURCE
VERTICAL WRITE CURRENT SOURCE
SELECTED HORIZONTAL WRITE DRIVE WHA-WHD, HORIZONTAL WRITE CURRENT HW0-HW3
SELECTED VERTICAL WRITE DRIVE WVA-WVD, VERTICAL WRITE CURRENT VW0-VW3
EV7 (7-8-9)
EV6
EV5
EV4
EV3
EV2
EV1
EV0
VERTICAL DRIVE DECK
BIT 9
BIT 8
BIT 7
ADDRESS BITS
VERTICAL DRIVE SELECT
REF
PWR
+4V
+4V
NOTE:
1. THE SA AND 9SA7 MODULES ARE FUNCTIONALLY IDENTICAL AND INTERCHANGEABLE.
CONTROL DATA
DEVELOPMENT DIVISION
9SA7 MODULE - SCM
READ/WRITE DRIVES AND
MEMORY STACK
CODE IDENT
C
DWG NO
60297600
REV
U
SHEET
PAGE
5-253

SENSE AMPLIFIERS

The 2SB7 module contains six Sense Amplifiers. Each amplifier circuit outputs a zero when all three inputs to the AND-NOT gate are ones. This will occur only when Sample Readout is present and neither of the Sense Signals is present. The circuit outputs a one at all other times. Even numbered test points correspond to the Sense Signal at odd numbered input pins, and vice versa.

INHIBIT DRIVES

The 2SB7 module contains four Vertical Inhibit Drives and three Horizontal Inhibit Drives. These circuits are enabled when the corresponding Inhibit Data Bit is set. Output current from each circuit is sent thru one of four inhibit wires. The selection is based on the condition of Address Bits 5 and 10 (for Vertical Inhibit Drives) and Address Bits 5 and 15 (for Horizontal Inhibit Drives).


BIT N+11 SENSE AMPL
BIT N+10 SENSE AMPL
BIT N+9 SENSE AMPL
BIT N+8 SENSE AMPL
BIT N+7 SENSE AMPL
BIT N+6 SENSE AMPL
EVEN STACK
ODD STACK
(9SA7) SENSE SIGNAL FROM EVEN (TOP) OR ODD (BOTTOM) MEMORY STACKS
READ DATA (SG)
(SE) SAMPLE READOUT
PARITY VERTICAL INHIBIT DRIVE
(SAME AS BIT N+6 EXCEPT D6 REPLACES DO)
BIT N+11 HORIZONTAL INHIBIT DRIVE
(SAME AS BIT N+6 EXCEPT D5 REPLACES DO)
BIT N+10 VERTICAL INHIBIT DRIVE
(SAME AS BIT N+6 EXCEPT D4 REPLACES DO)
BIT N+9 HORIZONTAL INHIBIT DRIVE
(SAME AS BIT N+6 EXCEPT D3 REPLACES DO)
BIT N+8 VERTICAL INHIBIT DRIVE
(SAME AS BIT N+6 EXCEPT D2 REPLACES DO)
BIT N+7 HORIZONTAL INHIBIT DRIVE
(SAME AS BIT N+6 EXCEPT D1 REPLACES DO)
J3 J2 J1 J0
K3 K2 K1 K0
BIT 15 PLANE SELECT (HORIZONTAL)
BIT 10 PLANE SELECT (VERTICAL)
BIT 5 STACK SELECT
(SF) ADDRESS BITS
INHIBIT DRIVE OUTPUT SELECT
NOTE:
1. THE 5B AND 2SB7 MODULES ARE FUNCTIONALLY IDENTICAL AND INTERCHANGEABLE.
INHIBIT DATA (SG)
INHIBIT CURRENT GENERATOR
BIT N+6 VERTICAL INHIBIT DRIVE
INHIBIT TRANSFORMER
ODD STACK HALF PLANE B
ODD STACK HALF PLANE A
EVEN STACK HALF PLANE B
EVEN STACK HALF PLANE A
(9SA7)

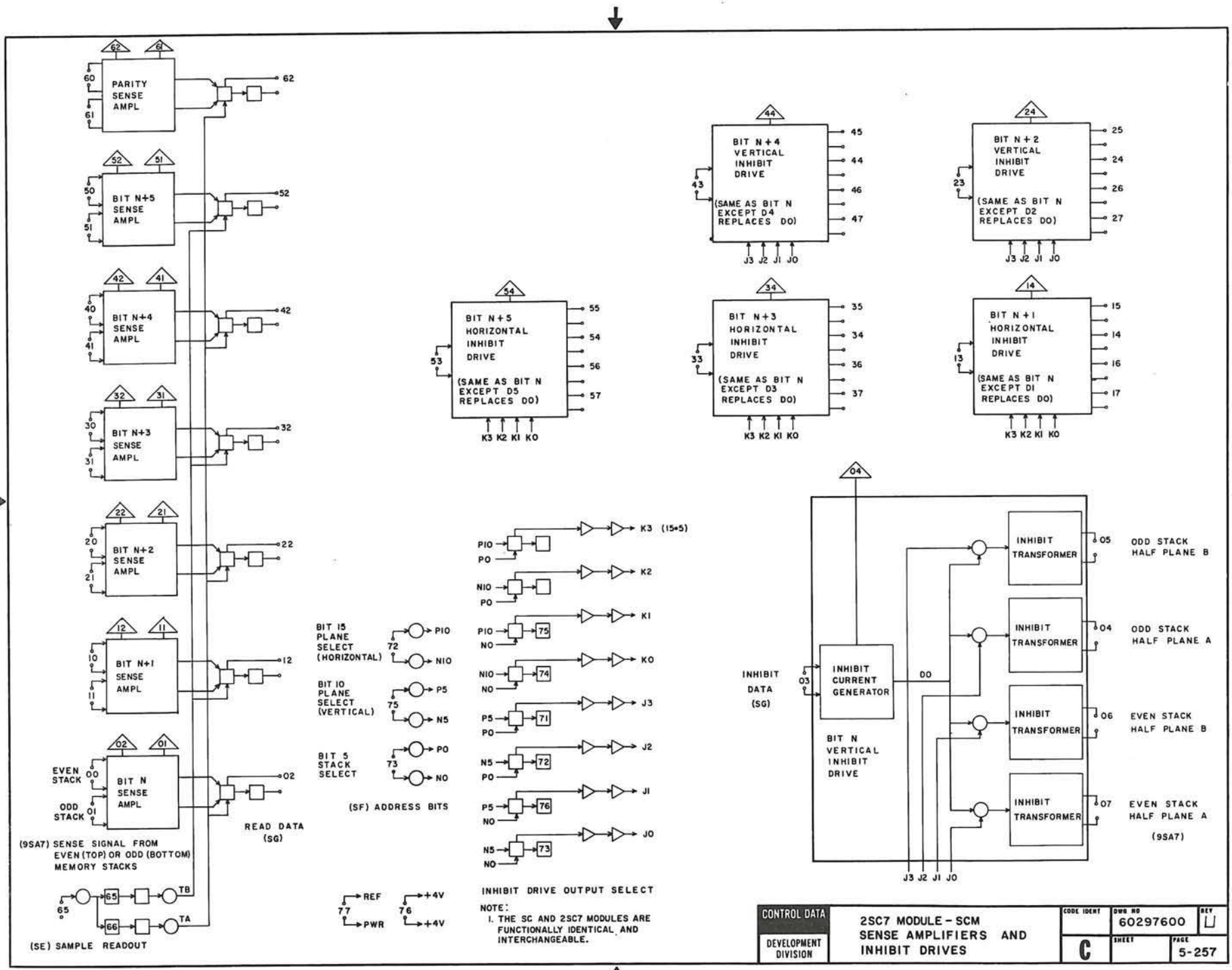
CONTROL DATA	2SB7 MODULE – SCM SENSE AMPLIFIERS AND INHIBIT DRIVES	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	
		SHEET	PAGE	5-255

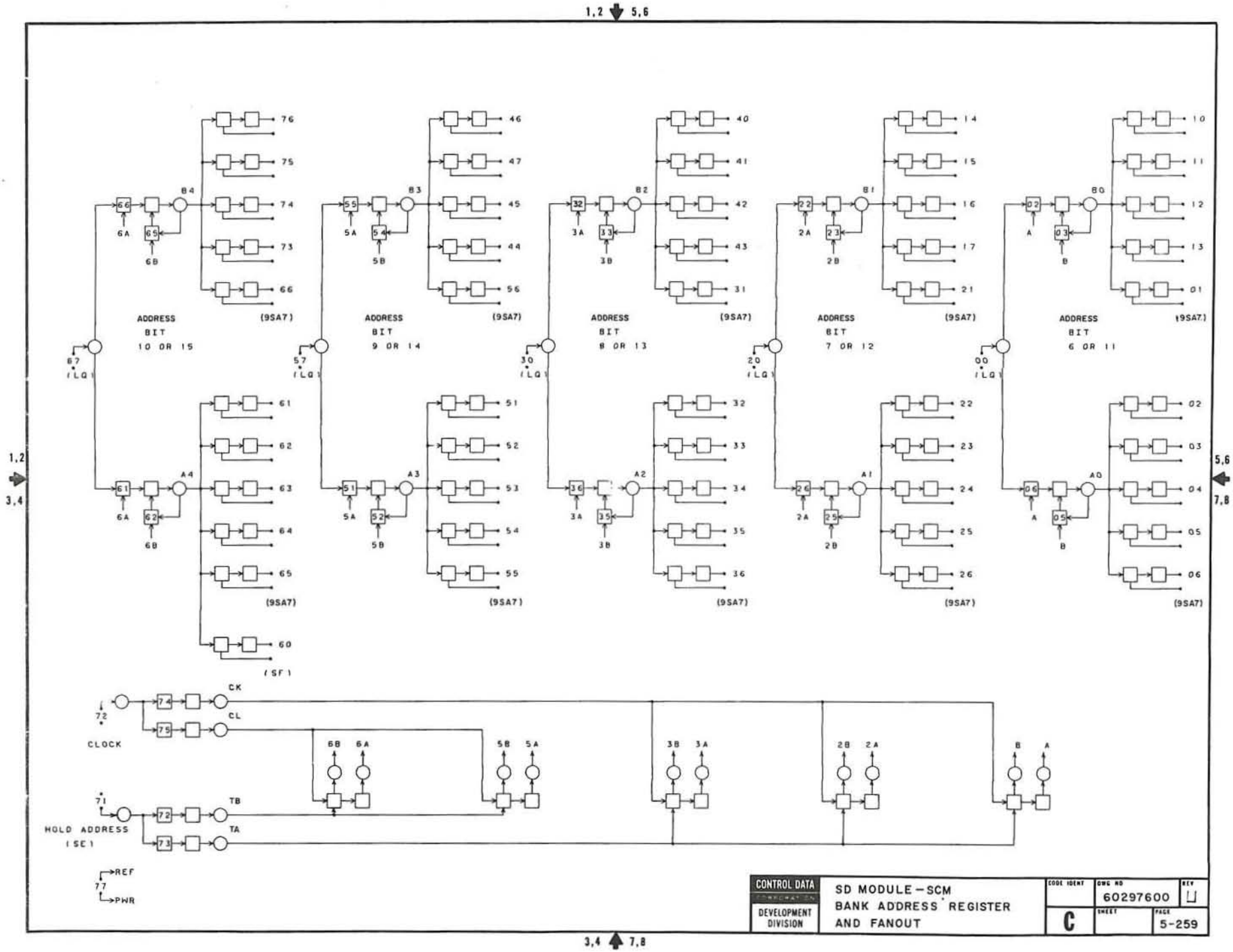
SENSE AMPLIFIERS

The 2SC7 module contains seven Sense Amplifiers. Each amplifier circuit outputs a zero when all three inputs to the AND-NOT gate are ones. This will occur only when Sample Readout is present and neither of the Sense Signals is present. The circuit outputs a one at all other times. Even numbered test points correspond to the Sense Signal at odd numbered input pins, and vice versa.

INHIBIT DRIVES

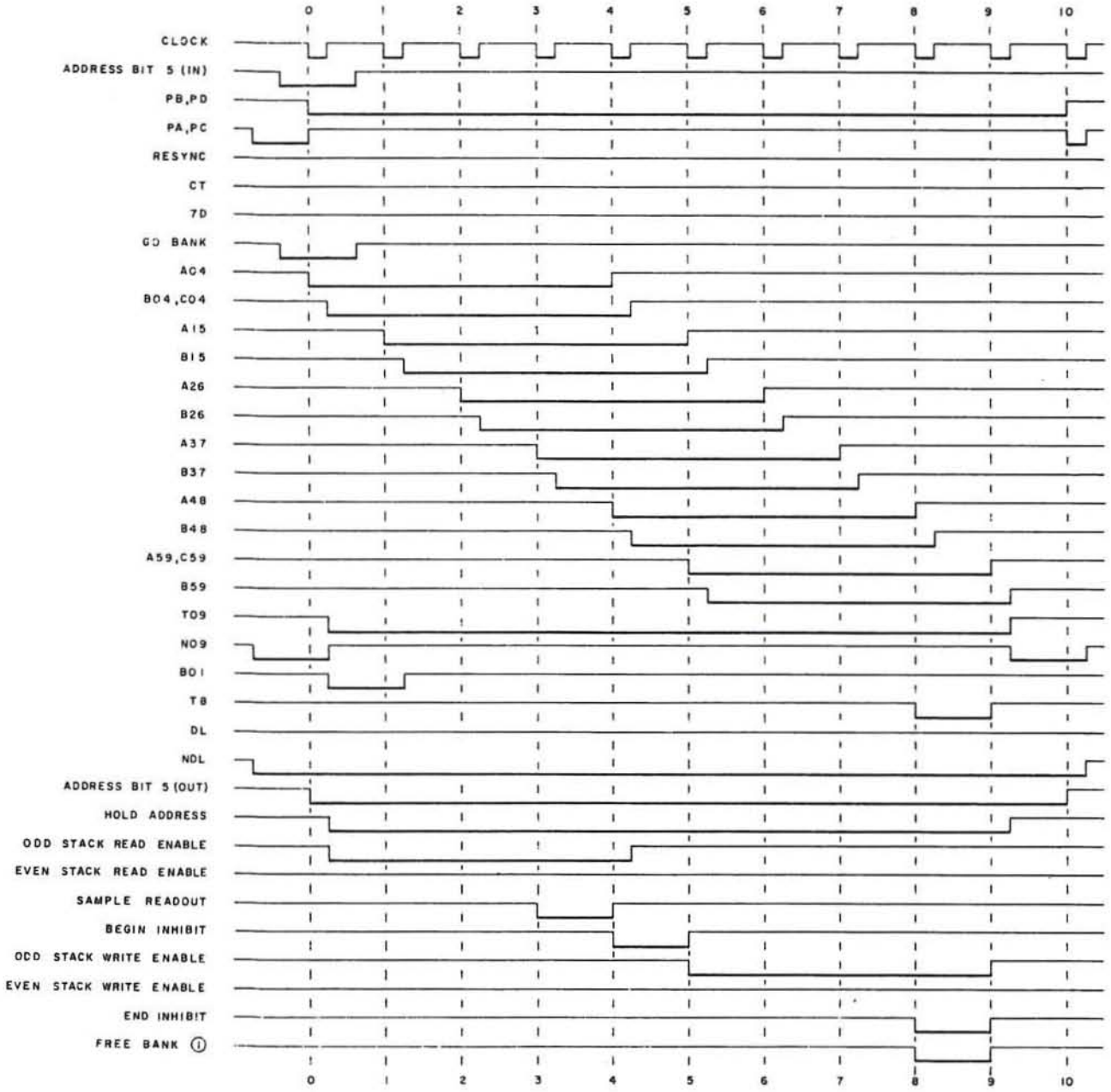
The 2SC7 module contains three Vertical Inhibit Drives and three Horizontal Inhibit Drives. These circuits are enabled when the corresponding Inhibit Data Bit is set. Output current from each circuit is sent thru one of four inhibit wires. The selection is based on the condition of Address Bits 5 and 10 (for Vertical Inhibit Drives) and Address Bits 5 and 15 (for Horizontal Inhibit Drives).


PARITY SENSE AMPL
BIT N+5 SENSE AMPL
BIT N+4 SENSE AMPL
BIT N+3 SENSE AMPL
BIT N+2 SENSE AMPL
BIT N+1 SENSE AMPL
BIT N SENSE AMPL
EVEN STACK
ODD STACK
(9SA7) SENSE SIGNAL FROM EVEN (TOP) OR ODD (BOTTOM) MEMORY STACKS
READ DATA (SG)
(SE) SAMPLE READOUT
BIT N+4 VERTICAL INHIBIT DRIVE
(SAME AS BIT N EXCEPT D4 REPLACES D0)
BIT N+2 VERTICAL INHIBIT DRIVE
(SAME AS BIT N EXCEPT D2 REPLACES D0)
BIT N+5 HORIZONTAL INHIBIT DRIVE
(SAME AS BIT N EXCEPT D5 REPLACES D0)
BIT N+3 HORIZONTAL INHIBIT DRIVE
(SAME AS BIT N EXCEPT D3 REPLACES D0)
BIT N+1 HORIZONTAL INHIBIT DRIVE
(SAME AS BIT N EXCEPT D1 REPLACES D0)
BIT 15 PLANE SELECT (HORIZONTAL)
BIT 10 PLANE SELECT (VERTICAL)
BIT 5 STACK SELECT
(SF) ADDRESS BITS
INHIBIT DRIVE OUTPUT SELECT
NOTE:
1. THE SC AND 2SC7 MODULES ARE FUNCTIONALLY IDENTICAL AND INTERCHANGEABLE.
INHIBIT DATA (SG)
INHIBIT CURRENT GENERATOR
BIT N VERTICAL INHIBIT DRIVE
INHIBIT TRANSFORMER
ODD STACK HALF PLANE B
ODD STACK HALF PLANE A
EVEN STACK HALF PLANE B
EVEN STACK HALF PLANE A
(9SA7)
CONTROL DATA
DEVELOPMENT DIVISION
2SC7 MODULE - SCM SENSE AMPLIFIERS AND INHIBIT DRIVES
CODE IDENT C
DWG NO 60297600
REV U
SHEET
PAGE 5-257


1,2
5,6
3,4
7,8
ADDRESS BIT 10 OR 15
ADDRESS BIT 9 OR 14
ADDRESS BIT 8 OR 13
ADDRESS BIT 7 OR 12
ADDRESS BIT 6 OR 11
(9SA7)
(SF)
CLOCK
HOLD ADDRESS
(SE)
CK
CL
TB
TA
REF
PWR
CONTROL DATA
DEVELOPMENT DIVISION
SD MODULE – SCM
BANK ADDRESS REGISTER
AND FANOUT
CODE IDENT
C
DWG NO
60297600
REV
SHEET
PAGE
5-259

SE MODULE

TIMING DIAGRAM



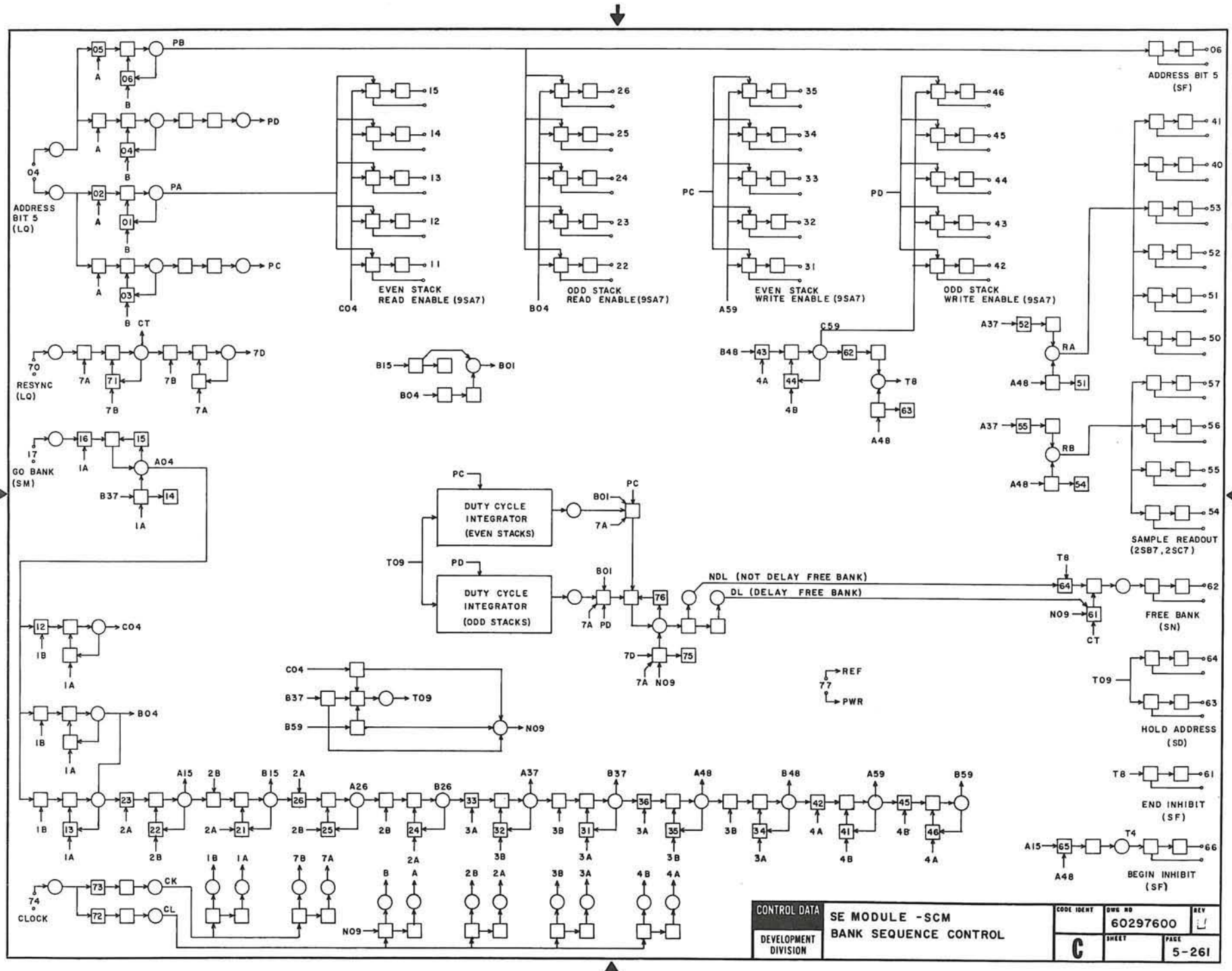
TRANSLATIONS

CLOCK- PULSE NUMBERS BEGIN WHEN GO BANK ARRIVES.
ADDRESS BIT 5 (IN): ARBITRARILY SHOWN SET WHEN GO BANK ARRIVES AND CLEAR AT ALL OTHER TIMES.
PB, PD (START): ADDRESS BIT 5 • N09 • CLOCK.
PB, PD (END): $\overline{\text{ADDRESS BIT 5}}$ • N09 • CLOCK.
PA, PC (START): $\overline{\text{ADDRESS BIT 5}}$ • N09 • CLOCK.
PA, PC (END): ADDRESS BIT 5 • N09 • CLOCK.
RESYNC: PRESENT ONCE EVERY 32 CLOCK PERIODS.
CT: RESYNC • CLOCK.
7D: CT • $\overline{\text{CLOCK}}$.
GO BANK: INITIATES BANK TIMING CHAIN.
A04 – B59: SET OUTPUTS OF BANK TIMING CHAIN.
T09: C04 + B37 + B59.
N09: $\overline{\text{C04}}$ • $\overline{\text{B37}}$ • $\overline{\text{B59}}$.
B01: B04 • $\overline{\text{B15}}$
T8: $\overline{\text{A48}}$ • C59
DL (START): ODD OR EVEN STACK DUTY CYCLE INTEGRATOR ACTIVATED • B01 • CLOCK.
DL (END): 7D • N09 • CLOCK.
NDL: $\overline{\text{DL}}$.
ADDRESS BIT 5 (OUT): PB.
HOLD ADDRESS: T09.
ODD STACK READ ENABLE: PB • B04.
EVEN STACK READ ENABLE: PA • C04.
SAMPLE READOUT: A37 • $\overline{\text{A48}}$.
BEGIN INHIBIT: A15 • A48.
ODD STACK WRITE ENABLE: PD • C59.
EVEN STACK WRITE ENABLE: PC • A59.
END INHIBIT: T8.
FREE BANK ①: T8 • NDL + CT • N09 • DL.

NOTE:

① FREE BANK OUTPUT SIGNAL WILL BE DELAYED IF ODD OR EVEN STACK DUTY CYCLE INTEGRATOR (DCI) IS ACTIVE. THIS CIRCUIT PREVENTS REPETITIVE REFERENCING OF THE ODD OR EVEN STACK IN A BANK. THE FOLLOWING DCI CHARACTERISTICS ARE FOR SPECIFIC CASES AND WILL VARY DEPENDING ON THE REFERENCE RATE:

1. DCI WILL ACTIVATE AFTER 100% REFERENCING FOR 200 USEC OR 50% REFERENCING FOR 400 USEC.
2. AFTER DCI IS ACTIVE AND 100% REFERENCING CONTINUES, THE FREE BANK SIGNAL WILL COINCIDE WITH THE RESYNC SIGNAL. THEREFORE, THE BANK READ/WRITE CYCLE TIME WILL BE 32 CLOCK PERIODS.
3. THE DCI REMAINS ACTIVE FOR APPROX 1 MS AFTER ALL BANK REFERENCES CEASE.


ADDRESS BIT 5 (LQ)
RESYNC (LQ)
GO BANK (SM)
CLOCK
EVEN STACK READ ENABLE (9SA7)
ODD STACK READ ENABLE (9SA7)
EVEN STACK WRITE ENABLE (9SA7)
ODD STACK WRITE ENABLE (9SA7)
ADDRESS BIT 5 (SF)
SAMPLE READOUT (2SB7, 2SC7)
DUTY CYCLE INTEGRATOR (EVEN STACKS)
DUTY CYCLE INTEGRATOR (ODD STACKS)
NDL (NOT DELAY FREE BANK)
DL (DELAY FREE BANK)
FREE BANK (SN)
HOLD ADDRESS (SD)
END INHIBIT (SF)
BEGIN INHIBIT (SF)
CONTROL DATA
DEVELOPMENT DIVISION
SE MODULE -SCM
BANK SEQUENCE CONTROL
CODE IDENT
C
DWG NO
60297600
REV
SHEET
PAGE
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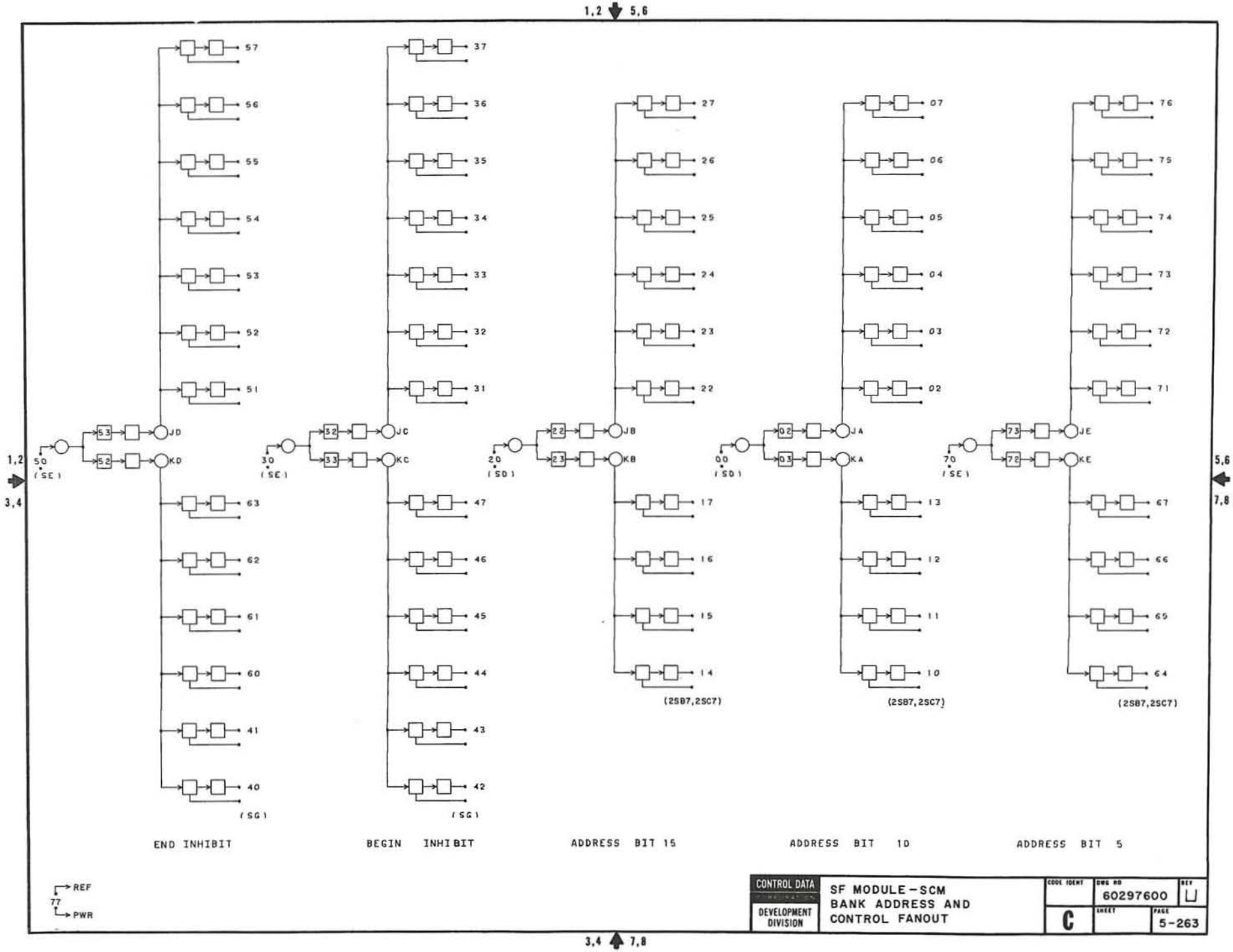
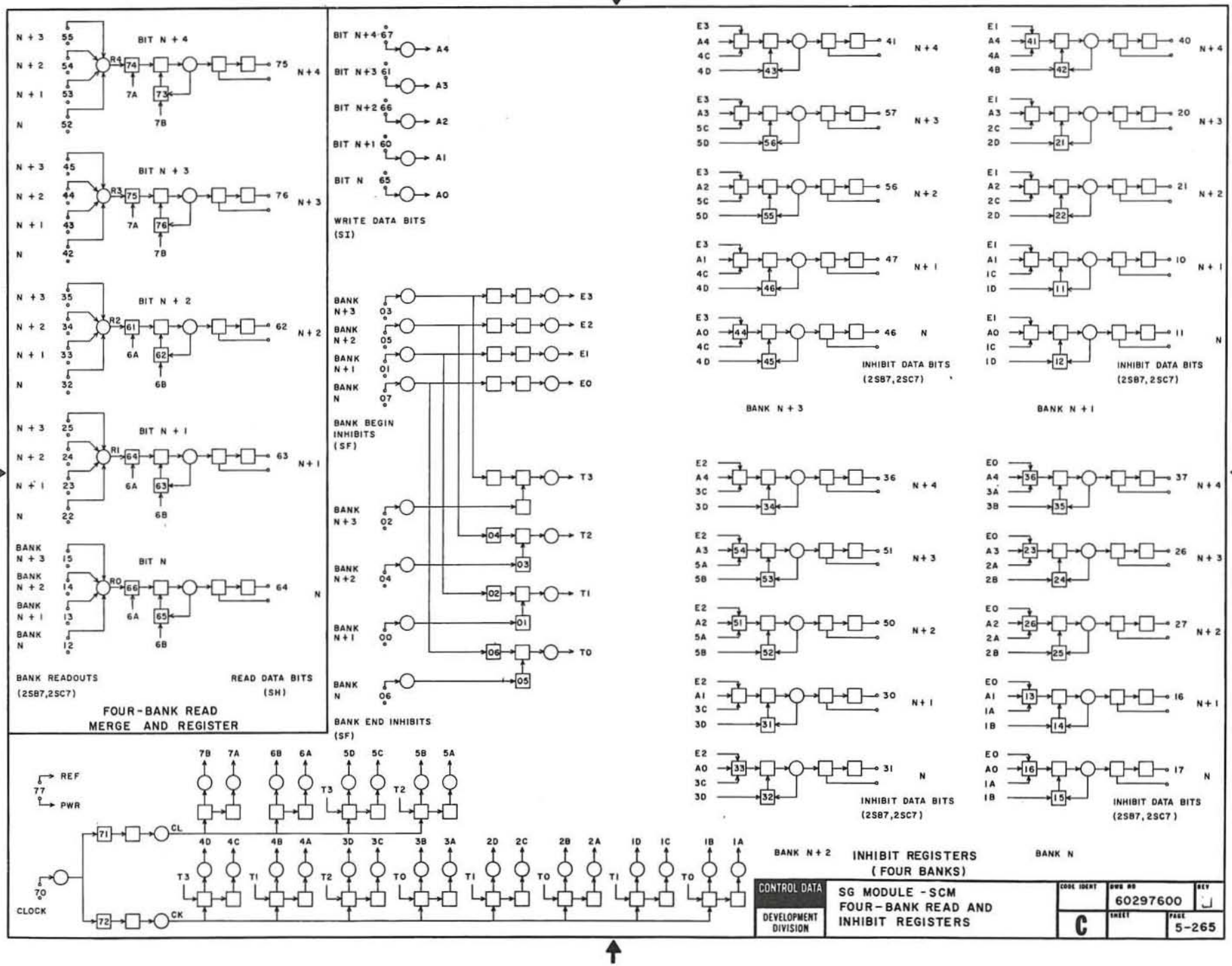

1,2
5,6
3,4
7,8
57
56
55
54
53
52
51
JD
KD
50
(SE)
63
62
61
60
41
40
(SG)
END INHIBIT
37
36
35
34
33
32
31
JC
KC
30
(SE)
47
46
45
44
43
42
(SG)
BEGIN INHIBIT
27
26
25
24
23
22
JB
KB
20
(SD)
17
16
15
14
(2SB7,2SC7)
ADDRESS BIT 15
07
06
05
04
03
02
JA
KA
00
(SD)
13
12
11
10
(2SB7,2SC7)
ADDRESS BIT 10
76
75
74
73
72
71
JE
KE
70
(SE)
67
66
65
64
(2SB7,2SC7)
ADDRESS BIT 5
REF
77
PWR
CONTROL DATA
DEVELOPMENT DIVISION
SF MODULE-SCM
BANK ADDRESS AND
CONTROL FANOUT
CODE IDENT
C
DWG NO
60297600
REV
U
SHEET
PAGE
5-263

FOUR-BANK READ MERGE AND REGISTER

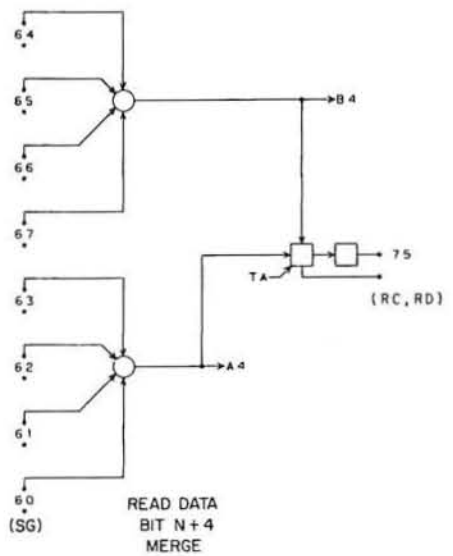
Each SG module contains five bits of a register which holds read data from one of four SCM Banks. If none of the banks is sending read data during a given clock period, all of the AND gates (R0-R4 terms) will be made. If one of the banks is sending read data, the AND gates will be either made or broken depending on the data. Therefore, these gates actually perform an OR function.

INHIBIT REGISTERS

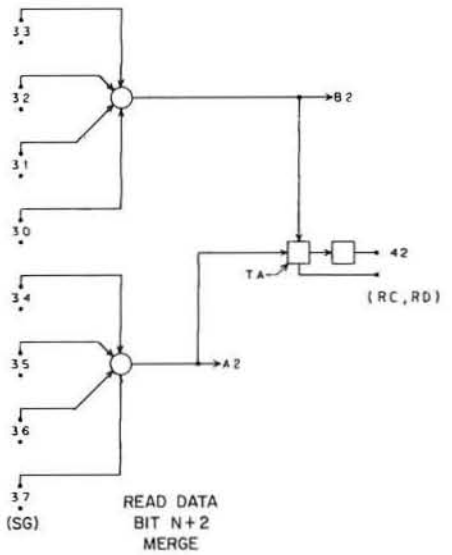
Each SG module contains a five-bit section for each of four Bank Inhibit Registers. Complemented write data enters one of these registers when the corresponding Bank Begin Inhibit signal is present. The selected register clears when the Bank End Inhibit signal appears five clock periods later.


BIT N+4
BIT N+3
BIT N+2
BIT N+1
BIT N
WRITE DATA BITS (SI)
BANK READOUTS (2S87,2SC7)
READ DATA BITS (SH)
FOUR-BANK READ MERGE AND REGISTER
BANK BEGIN INHIBITS (SF)
BANK END INHIBITS (SF)
INHIBIT DATA BITS (2S87,2SC7)
BANK N+3
BANK N+1
BANK N+2
BANK N
INHIBIT REGISTERS (FOUR BANKS)
REF
PWR
CLOCK
CL
CK
CONTROL DATA
DEVELOPMENT DIVISION
SG MODULE - SCM
FOUR-BANK READ AND INHIBIT REGISTERS
60297600
C
5-265

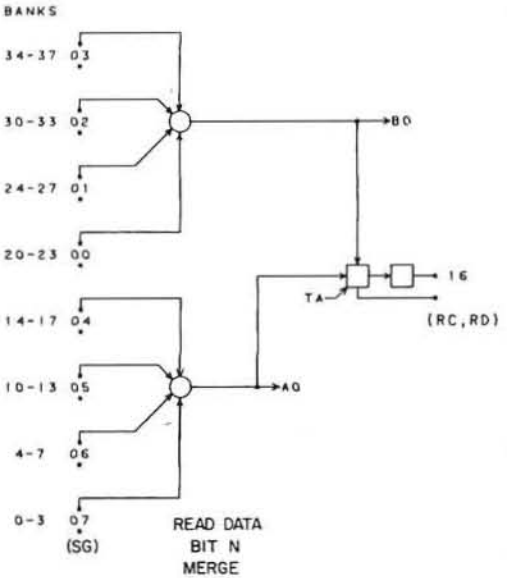
1,2 ⇩ 5,6



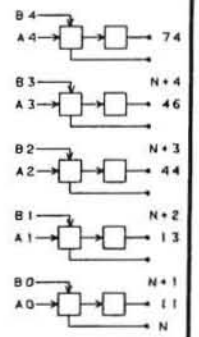
READ DATA BIT N+4 MERGE



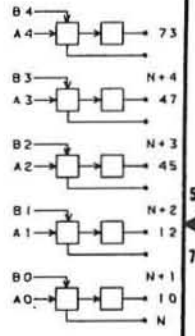
READ DATA BIT N+2 MERGE



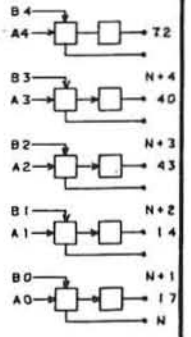
READ DATA BIT N MERGE



READ DATA BITS (HP)

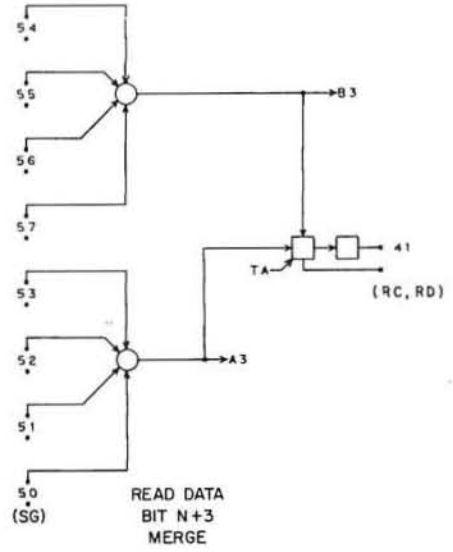


READ DATA BITS (HB)

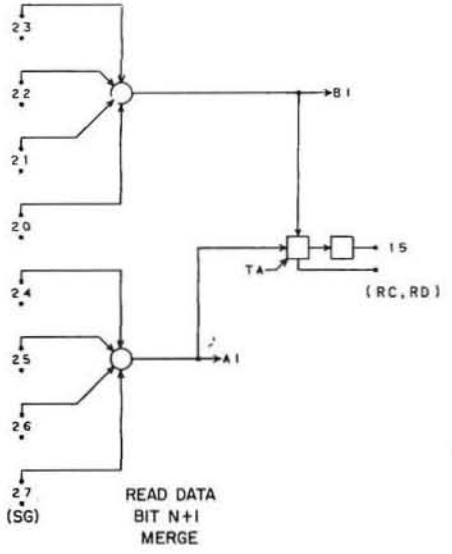


READ RESTORE DATA BITS (SI)

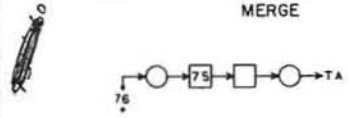
1,2 ⇩ 3,4



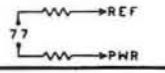
READ DATA BIT N+3 MERGE

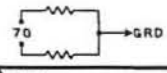


READ DATA BIT N+1 MERGE



READ SCM TO X (SI)

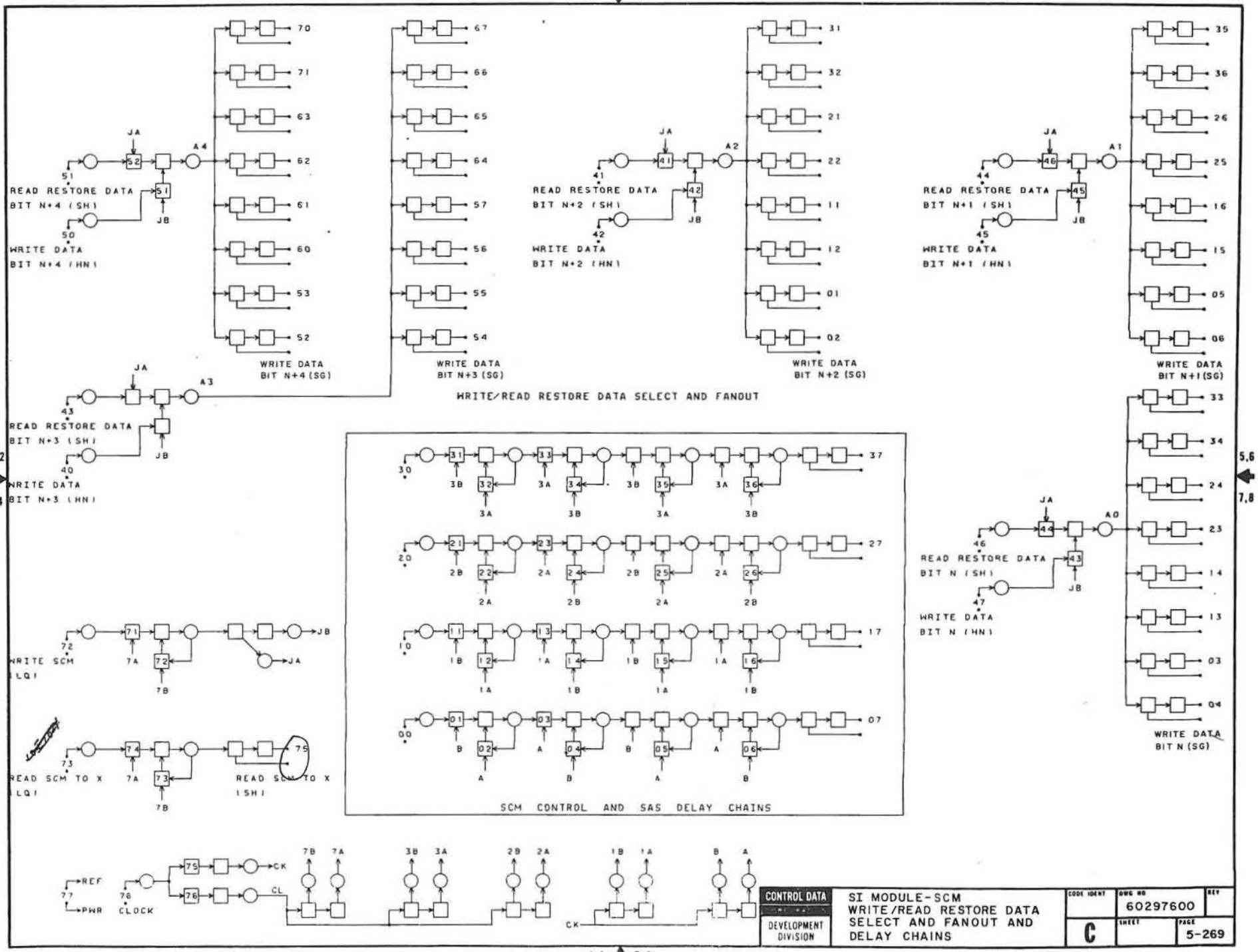




CONTROL DATA	SH MODULE-SCM READ DATA MERGE	CODE IDENT	DWG NO 60297600	REV
DEVELOPMENT DIVISION		C	SHEET	PAGE 5-267

3,4 ⇧ 7,8

1,2 ⇩ 5,6


READ RESTORE DATA BIT N+4 (SH)
WRITE DATA BIT N+4 (HN)
WRITE DATA BIT N+4 (SG)
READ RESTORE DATA BIT N+3 (SH)
WRITE DATA BIT N+3 (HN)
WRITE DATA BIT N+3 (SG)
READ RESTORE DATA BIT N+2 (SH)
WRITE DATA BIT N+2 (HN)
WRITE DATA BIT N+2 (SG)
READ RESTORE DATA BIT N+1 (SH)
WRITE DATA BIT N+1 (HN)
WRITE DATA BIT N+1 (SG)
READ RESTORE DATA BIT N (SH)
WRITE DATA BIT N (HN)
WRITE DATA BIT N (SG)
WRITE/READ RESTORE DATA SELECT AND FANOUT
WRITE SCM (LQ)
READ SCM TO X (LQ)
READ SCM TO X (SH)
SCM CONTROL AND SAS DELAY CHAINS
REF
PWR
CLOCK
CK
CL
1,2 ⇩ 3,4
5,6 ⇩ 7,8

CONTROL DATA DEVELOPMENT DIVISION	SI MODULE-SCM WRITE/READ RESTORE DATA SELECT AND FANOUT AND DELAY CHAINS	CODE IDENT C	DWG NO 60297600 REV SHEET PAGE 5-269

3,4 ⇧ 7,8

9JC7 MODULE

The 9JC7 module translates Destination Code Tag Bits 0-3 which are received from the SAS (SL module) during each clock period. As a result of this translation, one or more control signals are sent to the SCM, LCM, or CPU. These signals are delayed by timing chains of various lengths. The AND gates preceding the first FF of the timing chains are enabled by the Destination Code Tag Bits. For example, the shift stack timing chain (RS1-RS5 terms) is enabled when these bits equal 0001.

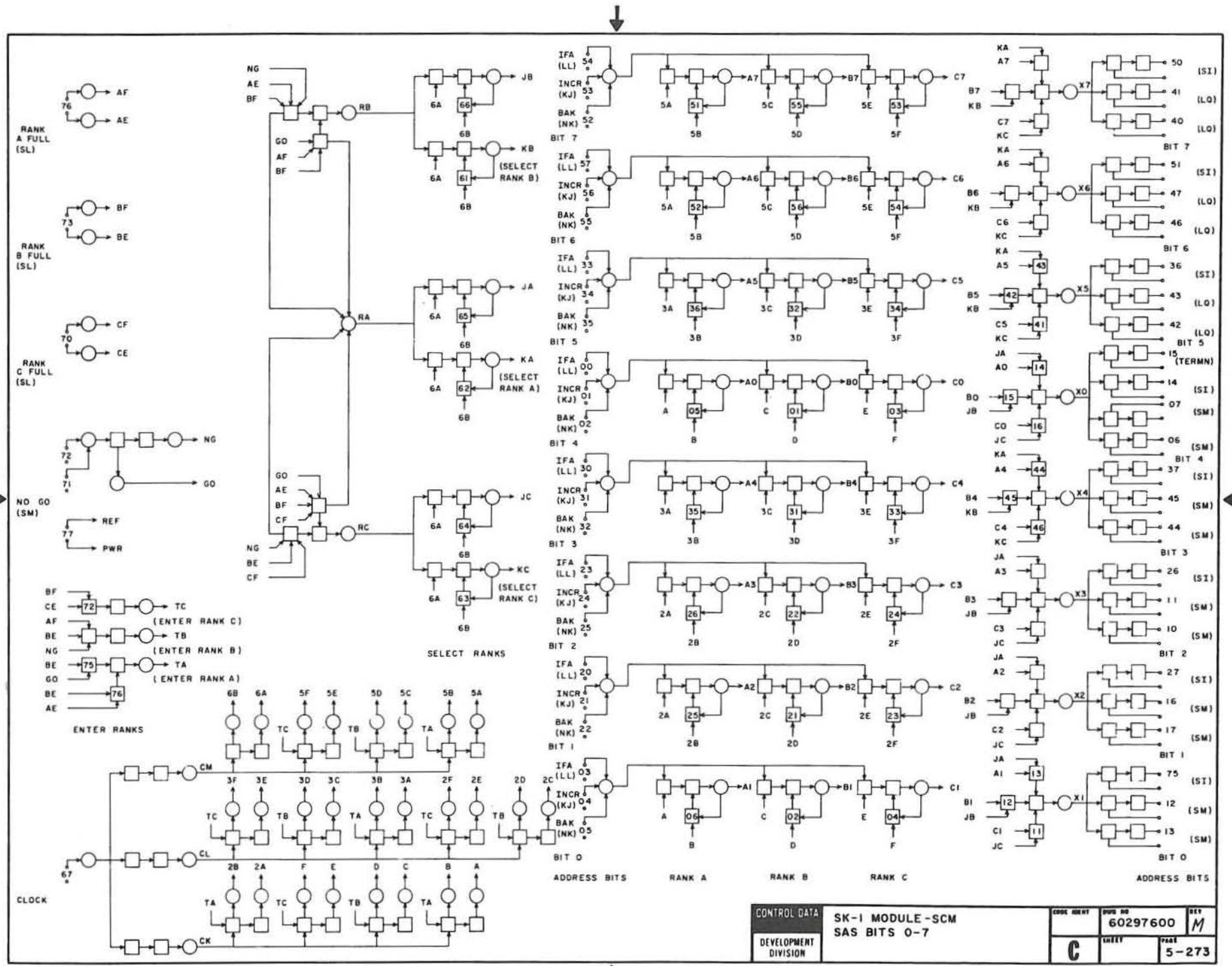
This page has been left blank intentionally. The SJ module has been replaced by the 9JC7 module.

SK-1 MODULE

The SK-1 module contains part of the SAS. Address Bits 0-7 from one of three sources (NK, KJ, or LL modules) are applied to the input AND gates. Only one of these sources will provide a meaningful input during a given clock period. The other two sources will send all ones. Therefore, these AND gates are actually performing OR functions. The address enters either Rank A, B, or C. An SAS rank is cleared and entered with an address during a clock period that the corresponding Enter Rank signal (TA, TB, TC terms) is present. The Enter Rank signals result from a translation of Rank A Full, Rank B Full, Rank C Full, and No Go input signals. These input signals are also used to determine which SAS rank is selected to send an address to the SCM Banks. This translation results in one of three pairs of clear-enter FFs being set during every clock period. The outputs of these FFs (JA, KA, JB, KB, JC, KC terms) are used to enable the outputs of the SAS ranks.

NOTE

The SK-1 and SK-2 modules are interchangeable.



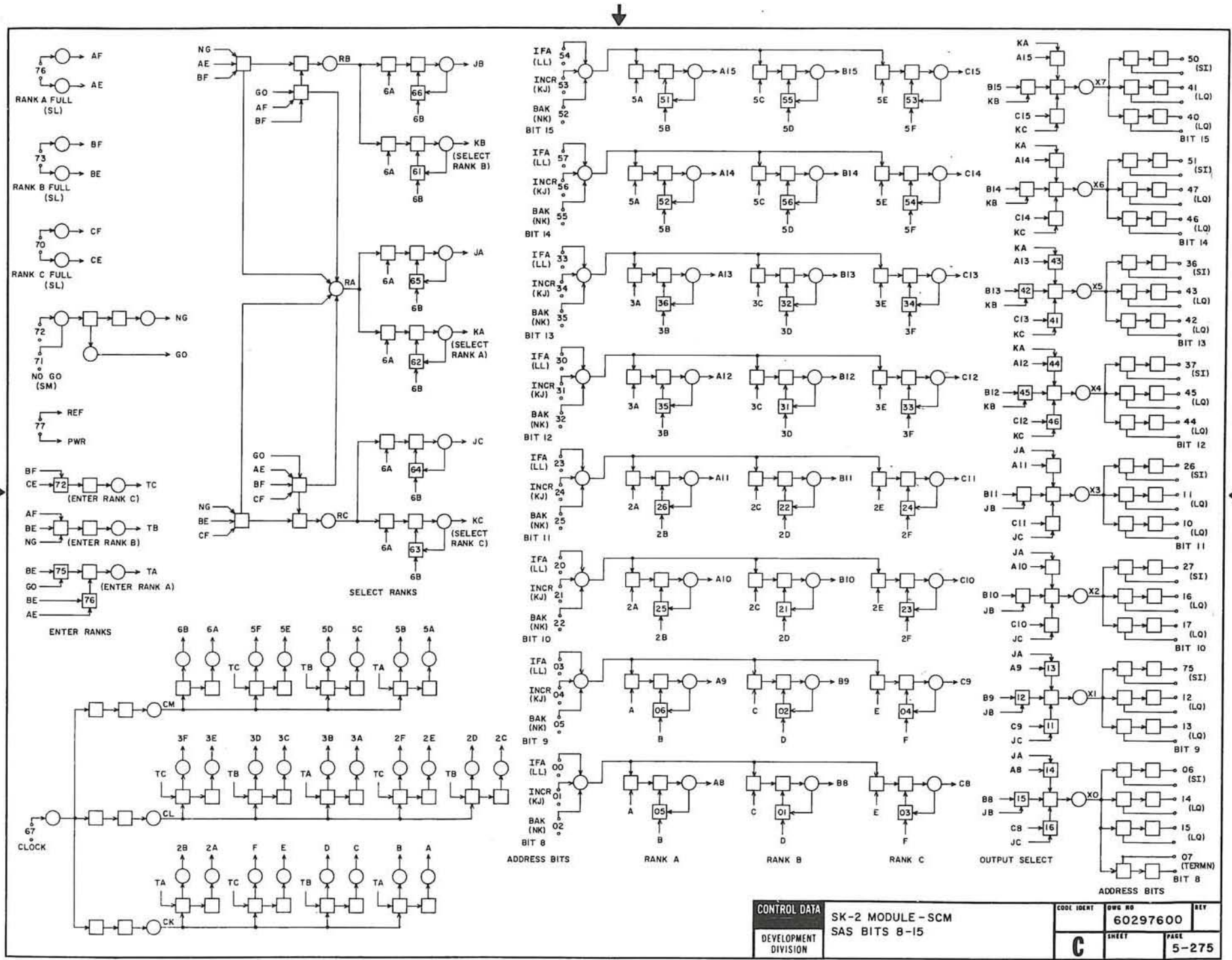
CONTROL DATA	SK-I MODULE-SCM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	SAS BITS 0-7	C	60297600	M
			SHEET	PAGE 5-273

SK-2 MODULE

The SK-2 module contains part of the SAS. Address Bits 8-15 from one of three sources (NK, KJ, or LL modules) are applied to the input AND gates. Only one of these sources will provide a meaningful input during a given clock period. The other two sources will send all ones. Therefore, these AND gates are actually performing OR functions. The address enters either Rank A, B, or C. An SAS rank is cleared and entered with an address during a clock period that the corresponding Enter Rank signal (TA, TB, TC terms) is present. The Enter Rank signals result from a translation of Rank A Full, Rank B Full, Rank C Full, and No Go input signals. These input signals are also used to determine which SAS rank is selected to send an address to the SCM Banks. This translation results in one of three pairs of clear-enter FFs being set during every clock period. The outputs of these FFs (JA, KA, JB, KB, JC, KC terms) are used to enable the outputs of the SAS ranks.

NOTE

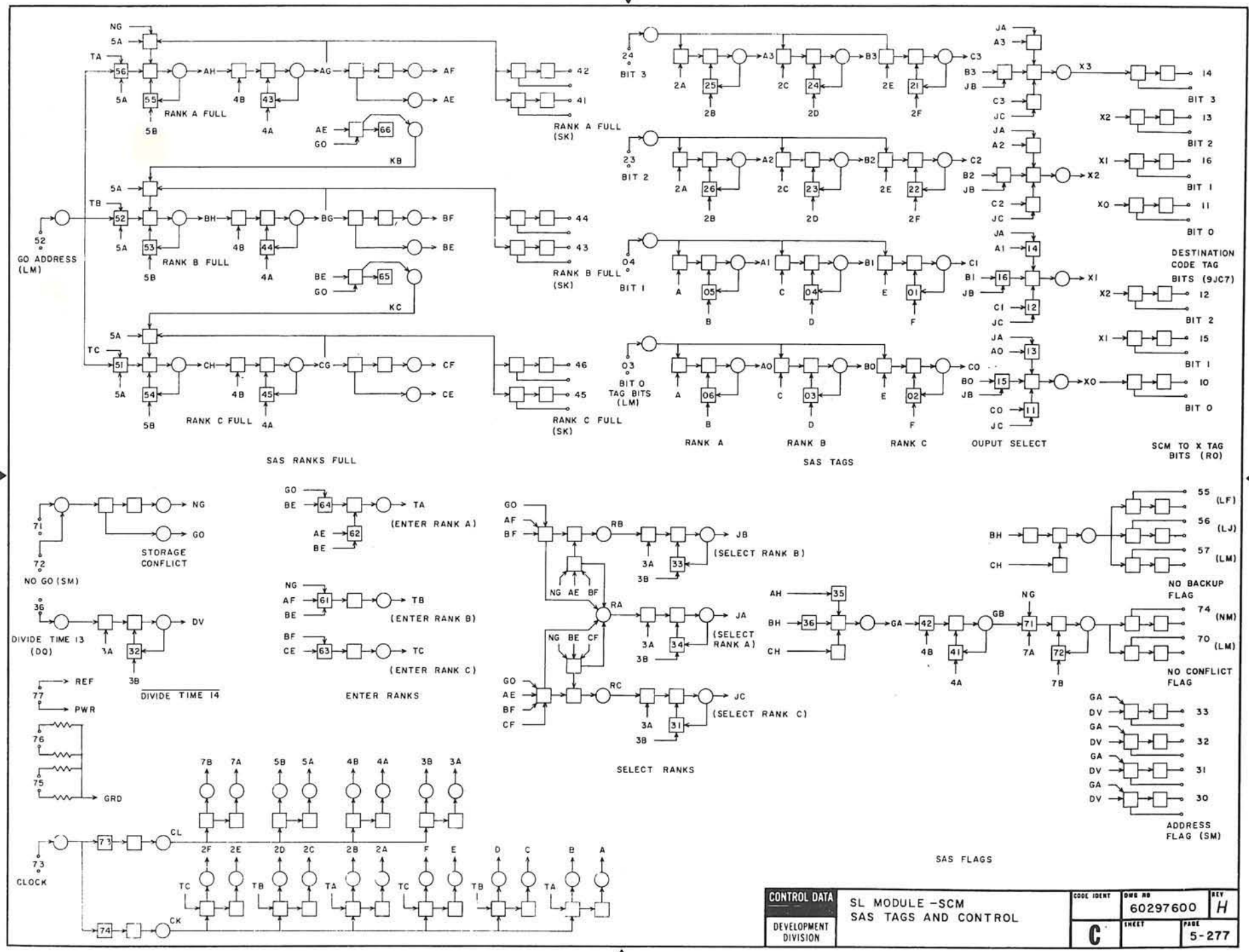
The SK-1 and SK-2 modules are interchangeable.



CONTROL DATA DEVELOPMENT DIVISION	SK-2 MODULE - SCM SAS BITS 8-15	CODE IDENT C	DWG NO 60297600	REV
			SHEET	PAGE 5-275

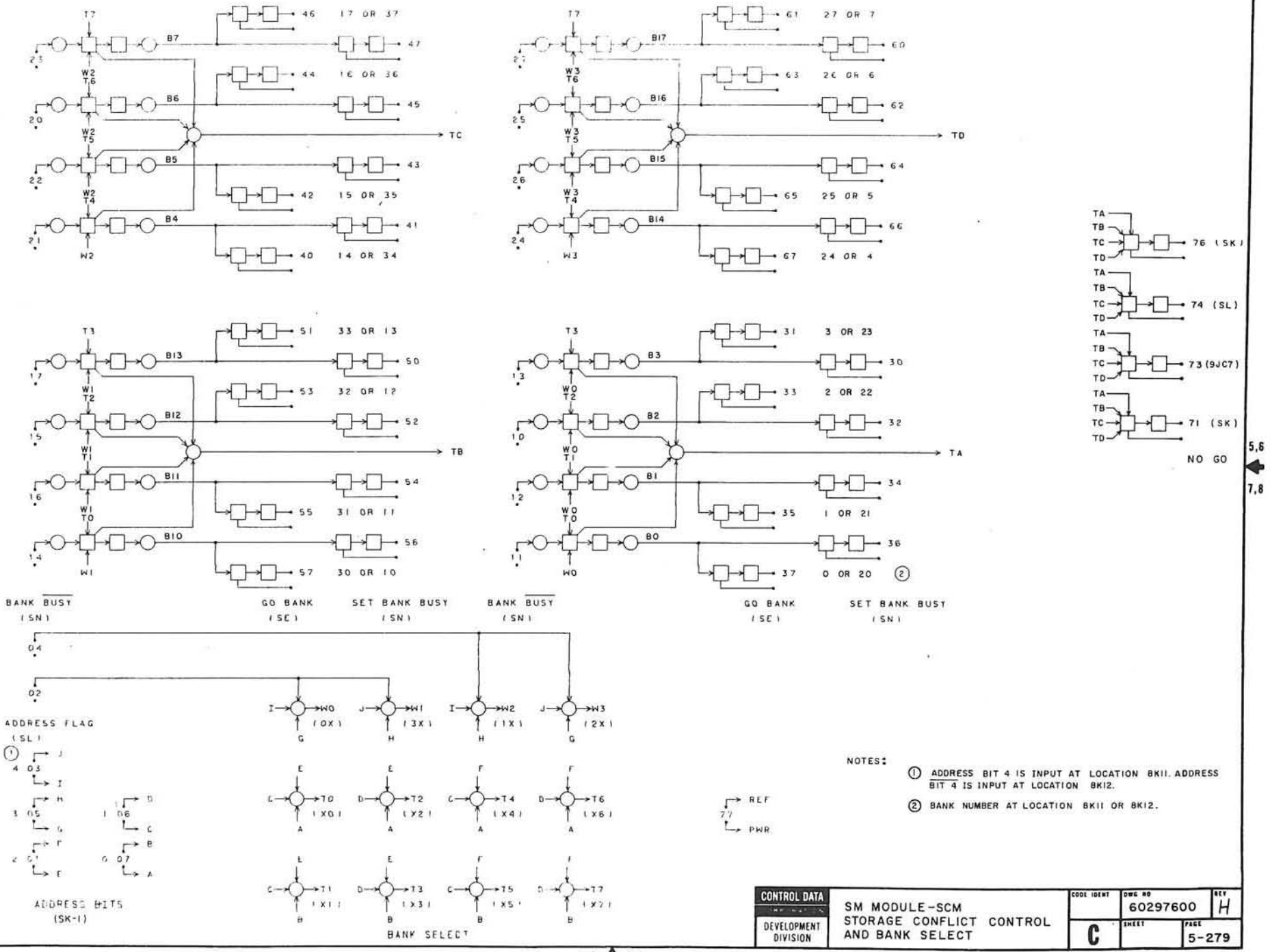
SL MODULE

The SL module contains part of the SAS. It also generates Rank A Full, Rank B Full, and Rank C Full control signals which are used by the entire SAS. Tag Bits 0-3 from the SCM Access Control (LM module) enter either Rank A, B, or C. An SAS rank is cleared and entered with the Tag Bits during a clock period that the corresponding Enter Rank signal (TA, TB, TC terms) is present. The Enter Rank signals result from a translation of Rank A Full, Rank B Full, Rank C Full, and No Go signals. These signals are also used to determine which SAS rank is selected to send the Tag Bits to SCM and CPU. This translation results in one of three FFs being set during every clock period. The outputs of these FFs (JA, JB, and JC terms) are used to enable the outputs of the SAS ranks.



CONTROL DATA	SL MODULE -SCM SAS TAGS AND CONTROL	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	H
			SHEET	PAGE 5-277

1,2 5,6


T7
B7
W2 T6
B6
W2 T5
B5
W2 T4
B4
W2
46 17 OR 37
47
44 16 OR 36
45
TC
43
42 15 OR 35
41
40 14 OR 34
T7
B17
W3 T6
B16
W3 T5
B15
W3 T4
B14
W3
61 27 OR 7
60
63 26 OR 6
62
TD
64
65 25 OR 5
66
67 24 OR 4
T3
B13
W1 T2
B12
W1 T1
B11
W1 T0
B10
W1
51 33 OR 13
50
53 32 OR 12
52
TB
54
55 31 OR 11
56
57 30 OR 10
T3
B3
W0 T2
B2
W0 T1
B1
W0 T0
B0
W0
31 3 OR 23
30
33 2 OR 22
32
TA
34
35 1 OR 21
36
37 0 OR 20 (2)
TA
TB
TC
TD
76 (SK)
74 (SL)
73 (9JC7)
71 (SK)
NO GO
1,2
3,4
5,6
7,8
BANK BUSY (SN)
GO BANK (SE)
SET BANK BUSY (SN)
BANK BUSY (SN)
GO BANK (SE)
SET BANK BUSY (SN)
04
02
ADDRESS FLAG (SL)
(1)
4 03
3 05
1 06
2 01
0 07
ADDRESS BITS (SK-1)
I W0 (0X)
J W1 (3X)
I W2 (1X)
J W3 (2X)
G
H
H
G
E T0 (X0)
D T2 (X2)
C T4 (X4)
D T6 (X6)
A
A
A
A
C T1 (X1)
D T3 (X3)
C T5 (X5)
D T7 (X7)
B
B
B
B
BANK SELECT
REF
77
PWR
NOTES:
(1) ADDRESS BIT 4 IS INPUT AT LOCATION 8K11. ADDRESS BIT 4 IS INPUT AT LOCATION 8K12.
(2) BANK NUMBER AT LOCATION 8K11 OR 8K12.
CONTROL DATA
DEVELOPMENT DIVISION
SM MODULE-SCM
STORAGE CONFLICT CONTROL
AND BANK SELECT
CODE IDENT
C
DWG NO
60297600
REV
H
SHEET
PAGE
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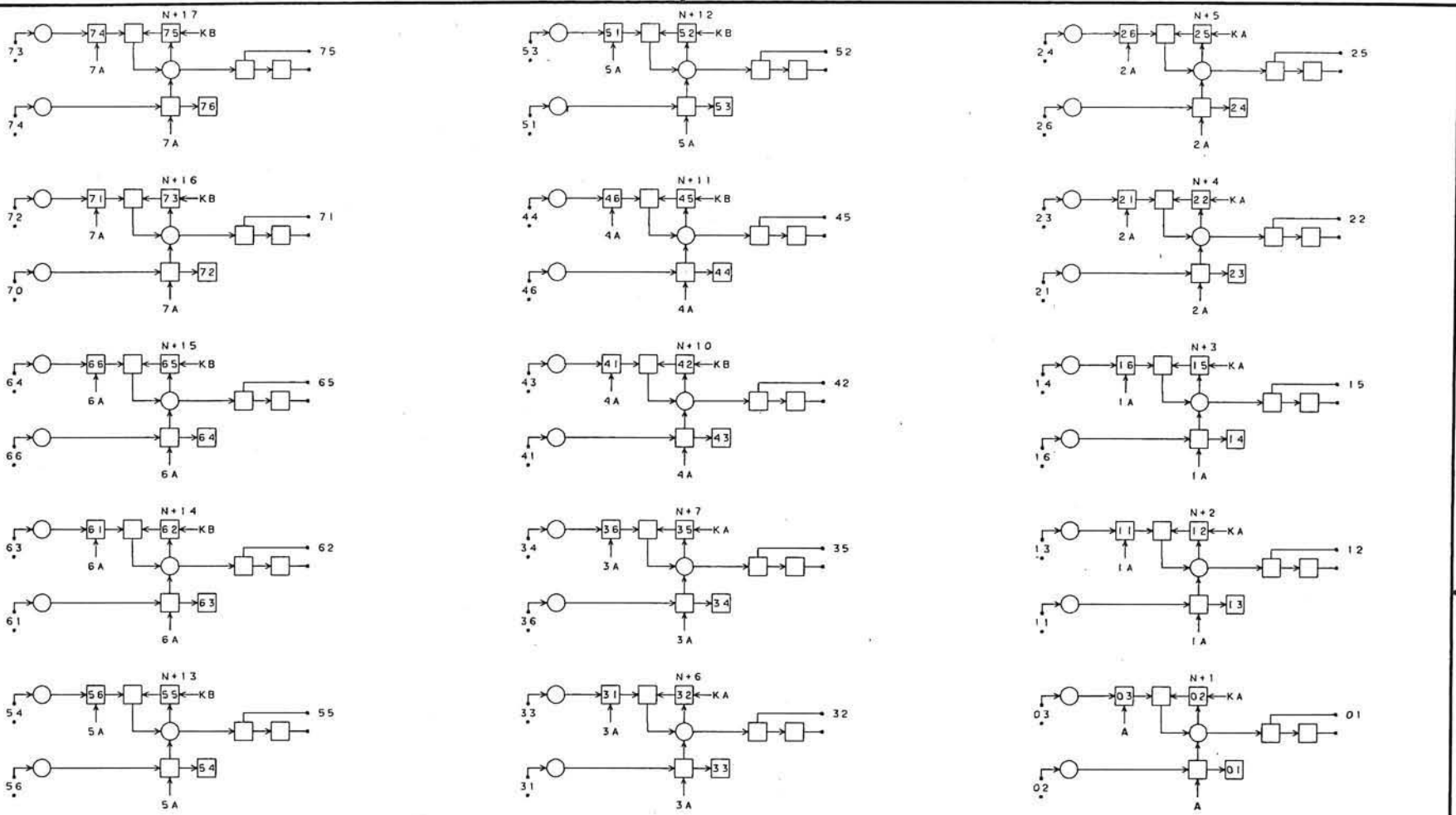
3,4 7,8

1,2 5,6



1,2 3,4 5,6 7,8

NOTE:
(1) ALSO APPLICABLE TO BANKS N+1 THROUGH N+17.

CONTROL DATA	SN MODULE-SCM BANK BUSY FLAGS	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	
		SHEET	PAGE	5-281

SECTION 5

PART 5

LARGE CORE MEMORY

PRIMARY BLOCK DIAGRAM
LARGE CORE MEMORY

The LCM is an eight-bank linear select type memory with a capacity of 512,000 64-bit words (including four odd parity bits per word). Each bank is independent of the other seven banks. A storage reference to a bank results in a read/write cycle which requires 64 clock periods to complete. Each bank has a 17 clock period access time from arrival of address to readout of data. Eight 64-bit words are simulaneously read from or written into a bank memory stack. These words are held in a 512-bit bank operand register. A subsequent reference to one of these words can be made without the delay of another read/write cycle. Maximum data transfer rate is one word each clock period. This occurs during block copies between SCM and LCM.

ADDRESS PATHS

ADDRESS ADDER

Three different types of 19-bit addresses are used to initiate an LCM storage reference. They are direct sequence addresses, initial block copy addresses, and subsequent block copy addresses. Each is formed by the Address Adder. In a Read LCM to X or Write X to LCM instruction, the address is formed by adding the lower 19 bits from the Xk Register to (RAL). In an LCM to SCM or SCM to LCM Block Copy instruction, the initial LCM address is formed by adding the lower 19 bits from the X0 Register to (RAL). All remaining addresses in a block copy are formed by the Pyramid Adder. This adder increases the initial address by one or ten (octal). An increase of one allows the next sequential word to be referenced. An increase of ten (octal) allows the next sequential bank to be referenced. The selected address is held in the Address Register.

BANK ADDRESS

Address Bits 6-18 are sent from the Address Register to all eight Bank Address Registers. However, this bank address will enter only one of these registers. These bits select a 512-bit word group, consisting of eight 64-bit words (including odd parity bits) from a selected bank. All words in the group are simultaneously read out or written into an LCM stack to or from a Bank Operand Register.

BANK SELECT

Address Bits 3-5 determine which one of the eight banks has been referenced.

WORD SELECT

Address Bits 0-2 determine which one of the eight words residing in a Bank Operand Register has been referenced.

PARITY ERROR ADDRESS

The LCM Parity Error Address Register holds the LCM address at which a parity error has occurred. Address Bits 0-5 enter from the Address Register. Address Bits 6-18 enter from one of the Bank Address Registers. The selection of the proper bank address is determined by Address Bits 3-5. If there are no Sections 0-3 Parity Errors, a new 19-bit address will enter every clock period. When an error occurs, the address at which the error occurred remains in the register for use by the MCU.

RANGE TESTS AND BLOCK COUNT

LCM DIRECT RANGE TEST

During a direct read or write instruction, the lowest order 19 bits of (Xk) are compared with (FLL) to determine if the requested address is in the assigned LCM field. If (Xk) is greater than or equal to (FLL), a flag will be set in the PSD Register. Also, if a direct write instruction was issued, the data will not be sent to LCM.

LCM BLOCK RANGE TEST

At the beginning of an LCM to SCM or SCM to LCM Block Copy instruction, a test is made to ensure that all requested addresses are in the assigned LCM field. The sum of K + (Bj) is added to the lowest order 19 bits of (X0). The resultant sum is compared

with (FLL). If greater than (FLL), indicating that the block copy will exceed the assigned LCM field, a flag will be set in the PSD Register and the instruction will not be executed.

SCM BLOCK RANGE TEST

At the beginning of an LCM to SCM or SCM to LCM Block Copy instruction, a test is made to ensure that all requested addresses are in the assigned SCM field. The sum of K + (Bj) is added to (A0). The resultant sum is compared with (FLS). If greater than (FLS), indicating that the block copy will exceed the assigned SCM field, a flag will be set in the PSD Register and the instruction will not be executed.

BLOCK COUNT CHECK

At the beginning of an LCM to SCM or SCM to LCM Block Copy instruction, the lowest order ten bits from the K + Bj Adder are gated into the Block Count Register. During each subsequent clock period, the block count is decremented by one. When the block copy is nearly complete, LCM Control is notified. If the original block count (K + Bj) is zero, the instruction will not be executed.

WRITE DATA PATHS

Data which is to be written into LCM enters Storage Register A from either an X Register or SCM. A parity bit is generated for each 15-bit section of the 60-bit word. The resultant 64 bits of data and parity are then transferred to Storage Register B. This register sends the information to a 64-bit word section of all eight Bank Operand Registers. Address Bits 3-5 determine which Bank Operand Register will be entered. Address Bits 0-2 determine which one of eight word sections of the register will be entered. If only one word is to be written, the remaining seven word sections are filled with sense data during the following bank read cycle. If all eight words (0-7) are to be written, the eight corresponding word sections will be entered with write data. This blocks entry of all sense data during the bank read cycle. All write and/or sense data in the Bank Operand Register is sent simultaneously to the Inhibit Generators during the bank write cycle.

READ DATA PATHS

During the bank read cycle, eight 64-bit words (including parity) are simultaneously read out of an LCM stack. The sense signals are amplified and sent to the Bank Operand Register. This sense data enters all word sections in which no write data was previously entered. Odd and even word read data from all eight Bank Operand Registers is merged in a Read Data Select and Fan-in network. The selected 60-bit (plus parity) word is entered into the Read Register. This word (less parity) is also sent to an X Register. Data in the Read Register is sent to SCM and to the Group Parity Check network. The Group and Section Parity Check networks determine whether a parity error has occurred in any one of the four 15-bit sections of the word. The four results are entered in the LCM Parity Error Register which is monitored by the MCU. If an error occurs, a flag will be set in the PSD Register. Also, the error address will be sent to the MCU.

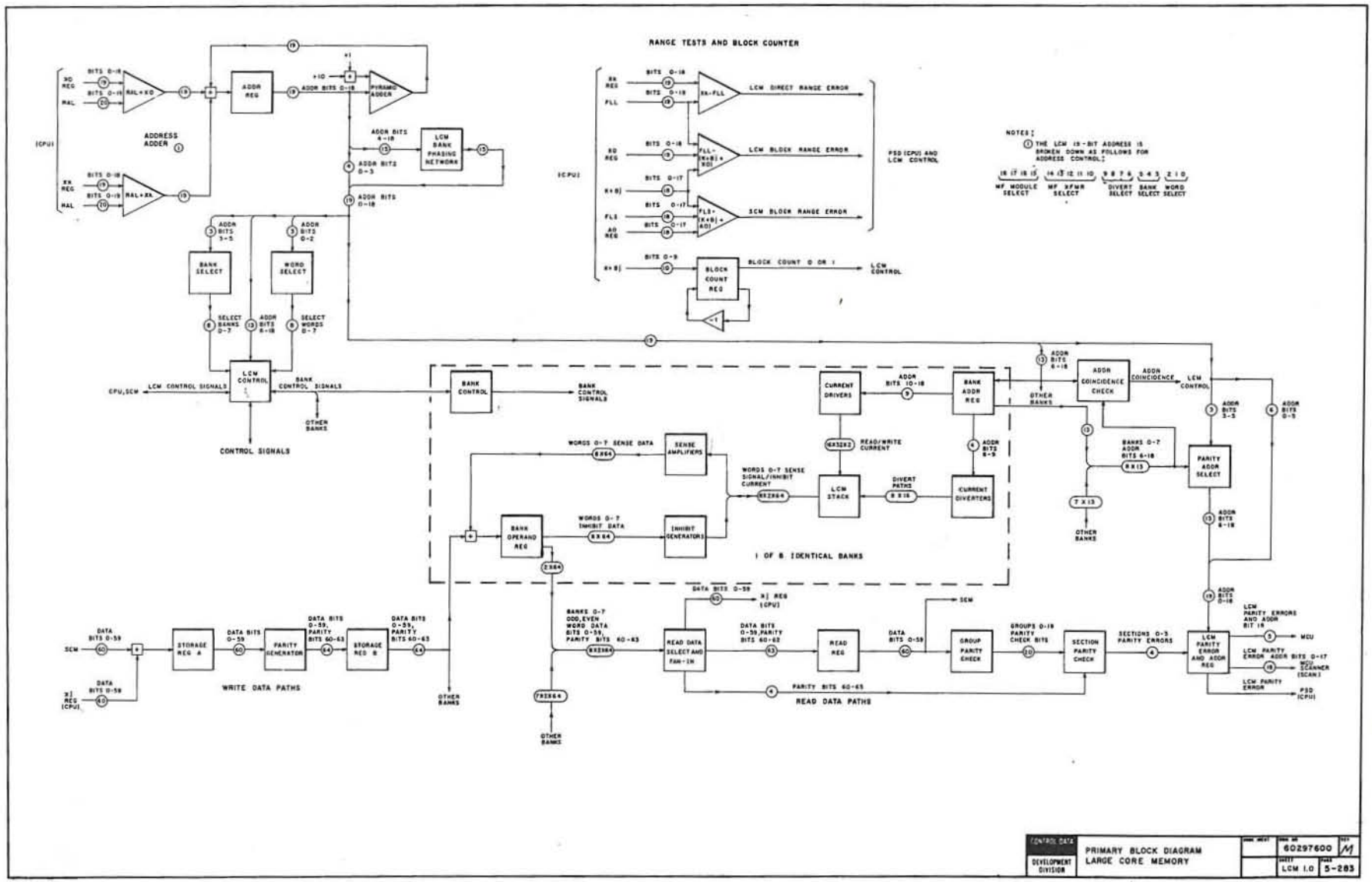
BANK READ/WRITE CYCLE

READ/SENSE

During the read portion of a bank read/write cycle, one Current Driver and eight Current Diverters are enabled. (Only one diverter circuit is actually involved.) This allows Read Current to flow thru one drive line. All cores (bits) along the drive line that are in a one state change to zeros. This change in state causes Sense Signals to be transmitted thru the sense/inhibit lines to the Sense Amplifiers. All cores that are in a zero state do not change. Therefore, no Sense Signals are generated. The Sense Amplifiers output Sense Data to the Bank Operand Register. After drive line data has been read from an LCM Stack, all cores in that location are in a zero state. However, the drive line data is restored during the write portion of the bank read/write cycle with the original data or new data.

WRITE/INHIBIT

During the write portion of the cycle, Write Current flows thru the read/write drive line in the opposite direction. Unless this current is unopposed, all cores along the drive line change to a one state. Where a zero state is required, Inhibit Current is passed thru the appropriate sense/inhibit line. This current opposes the Write Current. The resultant current is not sufficient to switch the core to a one state. Inhibit data is held in the Bank Operand Register. This data is the complement of write data and enables Bank Inhibit Generators to supply Inhibit Current to the sense/inhibit lines.



CONTROL DATA DEVELOPMENT DIVISION	PRIMARY BLOCK DIAGRAM LARGE CORE MEMORY	60297600 M
		SHEET LCM 1.0 PAGE 5-283

SECONDARY BLOCK DIAGRAM
DATA AND PARITY PATHS

SENSE/READ DATA PATH

Eight 64-bit (including four parity bits) data words are sensed simultaneously from a Bank Memory Stack during the read portion of the bank read/write cycle. These sense signals are amplified and complemented in the MA modules. The resultant data enters the appropriate Bank Operand Register (MB modules). Each of these modules contain four bits of the register for words 0, 2, 4, and 6 or for words 1, 3, 5, and 7. One odd word and one even word of read data are complemented and output simultaneously from all eight Bank Operand Registers to a Read Data Select and Fan-in network (ME and 1DC7 modules). The selected 60-bit (plus parity) word is then entered into the Read Register (MC modules). This word (less parity) is also sent to an X Register. Data in the Read Register is sent to SWF in SCM during the following clock period.

SENSE/READ DATA CONTROL

Sense data entering a Bank Operand Register is under the control of logic circuits and flags contained within the MR modules. Words 0-7 Sense Flags must all be set and Words 0-7 Write Flags must all be clear before all word sections of the register can be entered with sense data. The Sense Flags are all set when the Bank Sequence Control (MZ module) generates a Clear Write Flags signal. When the MZ module generates an Enter Sense signal, sense data is allowed to enter the word sections of the Bank Operand Register in which the corresponding Sense Flags are set and Write Flags are clear.

Read data leaving a Bank Operand Register is under the control of Odd and Even Bank Address Bits 1 and 2. These address bits are held in a register located in the ML modules. These modules also contain circuits which select the proper address source. RAL + Xk is selected for direct references; RAL + X0 is selected for the first word in a block copy; the pyramid is selected for all subsequent words in a block copy. When Pyramid Bit 0 is set and pyramid address has been selected, only odd Bank Operand Registers will receive address bits 1 and 2. When Pyramid Bit 0 is clear and pyramid address has been selected, only even registers will receive address bits 1 and 2.

Selection of the storage readout word in the ME and 1DC7 modules is determined by address bits 0, 3, 4, and 5 from the MS modules. When the Reduce Bank Count signal from the MT module is present during a 011 instruction, the octal value of bits 3-5 will be reduced by two. Data leaving LCM is dependent on gating signals at the destination registers.

WRITE/INHIBIT DATA PATH

Data which is to be written into a Bank Memory Stack originates at either an X Register or the SRO Register in SCM. The selected 60-bit word first enters Storage Register A (MD modules). One parity bit is formed for each 15-bit section of the 60-bit word in this register. In the following clock period, the 64 bits of data and parity are transferred to Storage Register B (MC and 1DC7 modules). This data (plus parity) is fanned-out in the following clock period to all eight Bank Operand Registers (MB modules). The data (plus parity) enters a selected register in a complemented form. Data enters the selected register one 60-bit (plus parity) word at a time under control of Write Flags. When data enters a word section of the Bank Operand Register, the corresponding word Sense Flag is cleared. This prevents entering sense data over the write data during the bank read cycle. This data is used during the write portion of a bank read/write cycle to activate Bank Inhibit Generators (MA modules). All 480 bits (plus parity) of inhibit data are transmitted to the MA modules simultaneously.

WRITE/INHIBIT DATA CONTROL

Write data entering Storage Register A is selected by Enter SCM Data and Enter Xj Data signals which are generated by the MV module. The data passes thru Storage Registers A and B in successive clock periods with no control signals required. Write data entering a Bank Operand Register is under control of Words 0-7 Write Flags (MR modules) which are individually set for one clock period. These flags are set by Address Bits 0-2 (word select) and Enter Write Flags and Select Bank Write Flags control signals (bank select). The corresponding word Sense Flag is cleared at this time. Inhibit data leaving a Bank Operand Register is under control of a Start Inhibit signal generated by the Bank Sequence Control.

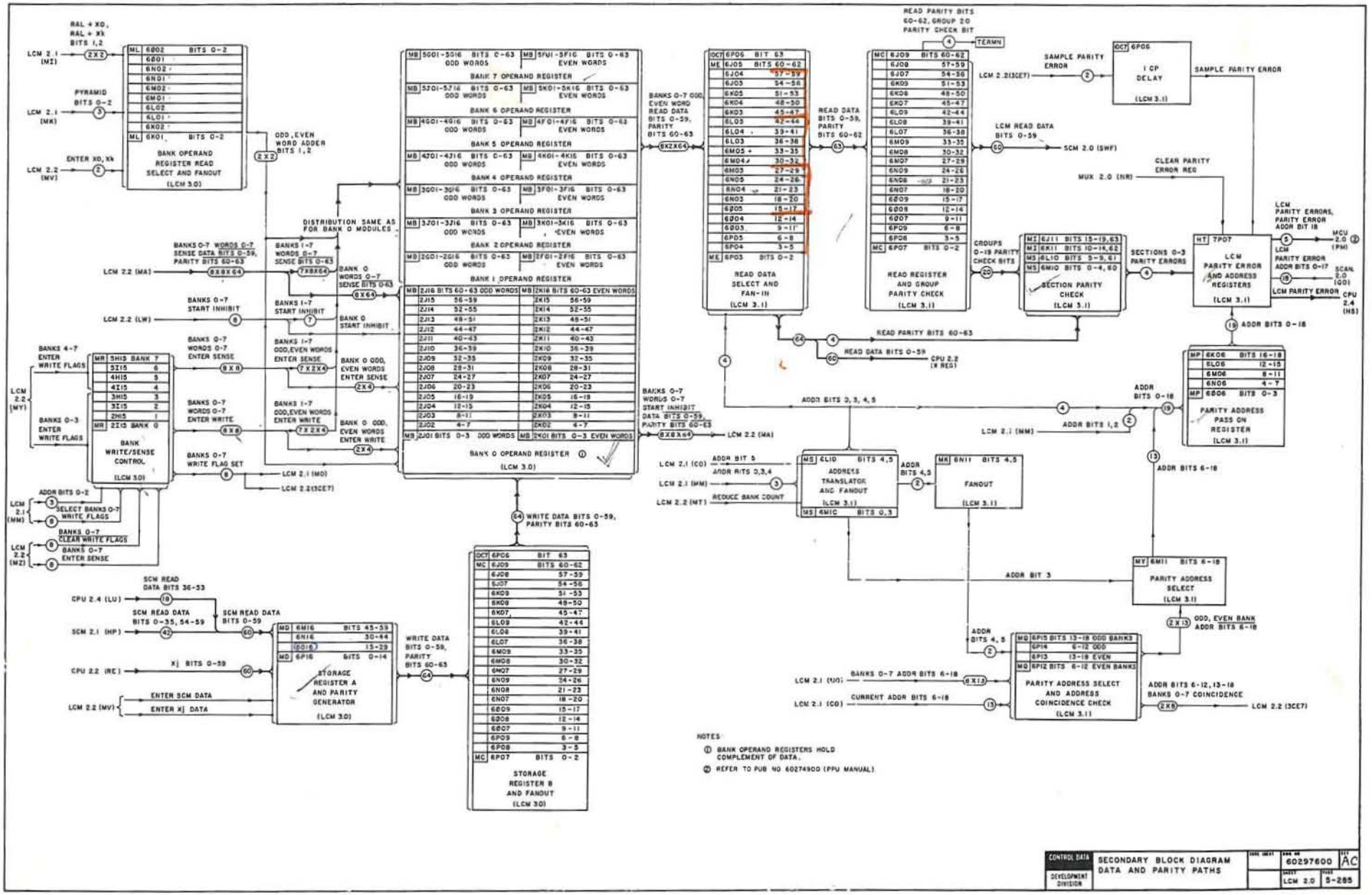
PARITY CHECK

The MC, MI, and MS modules contain circuits that check the four 15-bit sections of the word for errors that may have occurred during an LCM bank reference. The four results are entered into the LCM Parity Error Register (HT module). This register is monitored by the MCU. Each MC module contains three bits of the Read Register and a Group Parity Check circuit. This circuit checks the condition of the three-bit group in the register. These 20 bits are sent to four Section Parity Check circuits in the MI or MS modules. These circuits each check five Group Parity Check Bits. If odd parity exists (including applicable read parity bit), no Section Parity Error will be sent to the LCM Parity Error Register (HT module).

The HT module also contains a LCM Parity Error Address Register. This register holds the LCM address at which a parity error has occurred. LCM addresses are entered into this register every clock period if none of the LCM Parity Error Register bits are ones. When a parity error does occur, one or more of these bits will be a one. This blocks entry of any subsequent addresses in the LCM Parity Error Address Register. Address Bits 6-18 enter the register from a Bank Address Register (MO module) via MQ, MY, and MP modules. Address Bits 0, 3, 4, and 5 enter the register from the Address Holding Register (MM module) via MS and MP modules. Address Bits 1 and 2 enter the register from the Address Holding Register via an MP module. The selection of Address Bits 6-18 is dependent on the condition of Address Bits 3-5. These bits determine which Bank Address Register contains the parity error address.

ADDRESS COINCIDENCE CHECK

The MQ modules contain an Address Coincidence Check circuit. This circuit determines if a word stored in a Bank Memory Stack is also contained in the corresponding Bank Operand Register (MB modules) due to a previously issued instruction. A comparison is made between Current Address Bits 6-18 from the Bank Phasing Network (CO modules) and the address in each Bank Address Register (MO modules). If coincidence exists for the selected bank, a read/write cycle will not be initiated during a Read LCM to X (014) instruction. The word is transmitted directly from the Bank Operand Register to an X Register.


RAL + X0, RAL + Xk BITS 1,2
LCM 2.1 (MI)
PYRAMID BITS 0-2
LCM 2.1 (MK)
ENTER X0, Xk
LCM 2.2 (MV)
BANK OPERAND REGISTER READ SELECT AND FANOUT (LCM 3.0)
ODD, EVEN WORD ADDER BITS 1,2
BANK 7 OPERAND REGISTER
BANK 6 OPERAND REGISTER
BANK 5 OPERAND REGISTER
BANK 4 OPERAND REGISTER
BANK 3 OPERAND REGISTER
BANK 2 OPERAND REGISTER
BANK 1 OPERAND REGISTER
BANK 0 OPERAND REGISTER (1) (LCM 3.0)
DISTRIBUTION SAME AS FOR BANK 0 MODULES
BANKS 0-7 WORDS 0-7 SENSE DATA BITS 0-59, PARITY BITS 60-63
LCM 2.2 (MA)
BANKS 1-7 WORDS 0-7 SENSE BITS 0-63
BANK 0 WORDS 0-7 SENSE BITS 0-63
BANKS 0-7 START INHIBIT
LCM 2.2 (LW)
BANKS 1-7 START INHIBIT
BANK 0 START INHIBIT
BANKS 4-7 ENTER WRITE FLAGS
BANKS 0-3 ENTER WRITE FLAGS
LCM 2.2 (MY)
BANK WRITE/SENSE CONTROL (LCM 3.0)
BANKS 0-7 WORDS 0-7 ENTER SENSE
BANKS 1-7 ODD,EVEN WORDS ENTER SENSE
BANK 0 ODD, EVEN WORDS ENTER SENSE
BANKS 0-7 WORDS 0-7 ENTER WRITE
BANKS 1-7 ODD,EVEN WORDS ENTER WRITE
BANK 0 ODD, EVEN WORDS ENTER WRITE
BANKS 0-7 WRITE FLAG SET
LCM 2.1 (MO)
LCM 2.2 (3CE7)
ADDR BITS 0-2
LCM 2.1 (MM)
SELECT BANKS 0-7 WRITE FLAGS
BANKS 0-7 CLEAR WRITE FLAGS
LCM 2.2 (MZ)
BANKS 0-7 ENTER SENSE
SCM READ DATA BITS 36-53
CPU 2.4 (LU)
SCM READ DATA BITS 0-35, 54-59
SCM 2.1 (HP)
SCM READ DATA BITS 0-59
CPU 2.2 (RE)
Xj BITS 0-59
ENTER SCM DATA
ENTER Xj DATA
LCM 2.2 (MV)
STORAGE REGISTER A AND PARITY GENERATOR (LCM 3.0)
WRITE DATA BITS 0-59, PARITY BITS 60-63
WRITE DATA BITS 0-59, PARITY BITS 60-63
STORAGE REGISTER B AND FANOUT (LCM 3.0)
BANKS 0-7 ODD, EVEN WORD READ DATA BITS 0-59, PARITY BITS 60-63
READ DATA BITS 0-59, PARITY BITS 60-62
READ DATA SELECT AND FAN-IN (LCM 3.1)
READ PARITY BITS 60-62, GROUP 20 PARITY CHECK BIT
TERMN
READ REGISTER AND GROUP PARITY CHECK (LCM 3.1)
SAMPLE PARITY ERROR
LCM 2.2(3CE7)
1 CP DELAY (LCM 3.1)
SAMPLE PARITY ERROR
LCM READ DATA BITS 0-59
SCM 2.0 (SWF)
CLEAR PARITY ERROR REG
MUX 2.0 (NR)
GROUPS 0-19 PARITY CHECK BITS
SECTION PARITY CHECK (LCM 3.1)
SECTIONS 0-3 PARITY ERRORS
LCM PARITY ERROR AND ADDRESS REGISTERS (LCM 3.1)
LCM PARITY ERRORS, PARITY ERROR ADDR BIT 18
MCU 2.0 (2) (PM)
LCM PARITY ERROR ADDR BITS 0-17
SCAN 2.0 (QO)
LCM PARITY ERROR
CPU 2.4 (HS)
READ PARITY BITS 60-63
READ DATA BITS 0-59
CPU 2.2 (X REG)
ADDR BITS 0-18
PARITY ADDRESS PASS ON REGISTER (LCM 3.1)
ADDR BITS 0, 3, 4, 5
ADDR BITS 1,2
LCM 2.1 (NM)
BANKS 0-7 WORDS 0-7 START INHIBIT DATA BITS 0-59, PARITY BITS 60-63
LCM 2.2 (MA)
LCM 2.1 (CO)
ADDR BIT 5
ADDR BITS 0,3,4
LCM 2.1 (MM)
REDUCE BANK COUNT
LCM 2.2 (MT)
ADDRESS TRANSLATOR AND FANOUT (LCM 3.1)
ADDR BITS 4,5
FANOUT (LCM 3.1)
ADDR BITS 6-18
ADDR BIT 3
PARITY ADDRESS SELECT (LCM 3.1)
ODD, EVEN BANK ADDR BITS 6-18
ADDR BITS 4, 5
LCM 2.1 (UO)
BANKS 0-7 ADDR BITS 6-18
LCM 2.1 (CO)
CURRENT ADDR BITS 6-18
PARITY ADDRESS SELECT AND ADDRESS COINCIDENCE CHECK (LCM 3.1)
ADDR BITS 6-12, 13-18 BANKS 0-7 COINCIDENCE
LCM 2.2 (3CE7)
NOTES
(1) BANK OPERAND REGISTERS HOLD COMPLEMENT OF DATA.
(2) REFER TO PUB NO 60274900 (PPU MANUAL).
CONTROL DATA DEVELOPMENT DIVISION
SECONDARY BLOCK DIAGRAM DATA AND PARITY PATHS
60297600 AC
LCM 2.0 5-285

ADDRESS ADDER AND REGISTER

All LCM addresses are formed by the Address Adder. This two-stage adder is located within MI, MJ, MK, and MN modules. Address bits 4-18 are held in a Partial Sum Address Holding Register (MN modules). The lowest order bits are held in Address Bits 0-3 Holding Register (MM module). One of three types of addresses are entered into these registers. They are direct sequence addresses (RAL + Xk), initial block copy addresses (RAL + X0), and subsequent block copy addresses (Pyramid).

All but the first address in a block copy are formed by the Pyramid Adder (MK and MJ modules). This adder increases the initial address by 1 or 10 (octal) when a Go LCM or Advance 10 signal is present. A Go LCM signal indicates that an SCM address has been accepted in the SAS. This allows the next sequential LCM word to be referenced. An Advance 10 signal will be present during an LCM to SCM Block Copy instruction only. This allows the next sequential LCM Bank to be referenced.

BANK PHASING NETWORKS

Address Bits 4-18 pass thru a Bank Phasing Network before being used in LCM control. There are three different types of these networks. Each type requires a different set of CO modules.

When all eight LCM Banks are used, Address Bits 4-18 pass thru the network unchanged. The Banks 3 and 7 Busy signals from the Bank Select (3CE7 modules) are terminated. An 8-Bank Phase Enable signal is unconditionally sent to the SCM Access Control (LM module).

When LCM Banks 0-3 only are used, Address Bit 4 passes thru unchanged, Address Bit 5 is forced to zero, Address Bits 6-17 are shifted one bit position to the left and bit 18 is terminated. The Bank 3 Busy signal from the Bank Select (3CE7 module) is complemented and sent to the SCM Access Control (LM module). The Bank 7 Busy signal is terminated.

When LCM Banks 4-7 only are used, Address Bit 4 passes thru unchanged, Address Bit 5 is forced to one, Bits 6-17 are shifted one bit position to the left; bit 18 is terminated. The Bank 7 Busy signal from the Bank Select (3CE7 module) is complemented and sent to the SCM Access Control (LM module). The Bank 3 Busy signal is terminated.

BANK ADDRESS REGISTERS AND FANOUTS

The Bank Address Holding Register is contained in MX modules. Address Bits 6-18 arrive in a complemented form from the Bank Phasing Network (CO modules). This bank address is recomplemented before entering the register. The output of the Bank Address Holding Register is fanned-out to each individual Bank Address Register (MO modules). An address enters a selected register when the following conditions exist: Bank X Enter Address • (Block Mode Active + Bank X Write Flag Set). Bits 6-9 are sent to the MG modules (via LW and LX modules) where they select a Current Divert circuit. Bits 10-14 are sent to the MF modules (via LW modules) where they select a Current Driver circuit. The LX modules generate MF Module Read/Write Enable signals. These signals are dependent on the translation of bits 15-18 (MO modules) and Read/Write Enable signals from the selected Bank Sequence Control (MZ module). Each Bank Address Register also sends its output to the Address Coincidence Check circuit (MQ modules).

LCM DIRECT RANGE TEST

During a direct read or write (014 or 015) instruction, the lowest order 19 bits of (Xk) are compared with (FLL) to determine if the requested address is in the assigned LCM field. If (Xk) is greater than or equal to (FLL), the LCM Direct Range Condition Flag will be set in the PSD Register. Also, if a direct write instruction was issued, the data will not be sent to LCM.

Bits 0-18 from the FLL Register (HR modules) pass thru a fanout (MC modules) before entering the Xk-FLL circuit (MP modules). Bits 0-18 from the Xk Register (via MI and MJ modules) are gated by Enter Xk from the MV module. The Xk-FLL circuit generates Group Enables and Group Borrows which are sent to the LCM Direct Range Test circuit (MQ module). This circuit outputs a No Direct Range Error signal when Xk-FLL Range Error does not exist. This signal is sent to the 3CE7 modules via the MY module. When this signal is absent, the PSD Register (HS module) receives a LCM Direct Range Error signal if either of the Sample Direct Range signals is present.

LCM BLOCK RANGE TEST

At the beginning of an LCM to SCM or SCM to LCM Block Copy (011 or 012) instruction, a test is made to ensure that all requested addresses are in the assigned LCM field. The sum of K + (Bj) is added to the lowest order 19 bits of (X0). The resultant sum is compared with (FLL). If greater than (FLL), indicating that the block copy will exceed the assigned LCM field, the LCM Block Range Condition Flag will be set in the PSD Register and the instruction will not be executed.

Bits 0-18 from the X0 Register enter the FLL - (K + Bj + X0) circuit (MP modules) via the MI and MJ modules. Bits 0-17 from the K + Bj Adder (LV modules) enter the test circuit directly. Bits 0-18 from the FLL Register enter the test circuit via the MC modules. The FLL - (K + Bj + X0) circuit generates Group Enables and Group Borrows which are sent to the LCM Block Range Test circuit (MQ module). When this circuit detects an error, the PSD Register receives an LCM Block Range Error signal via the Block Control (MT module).

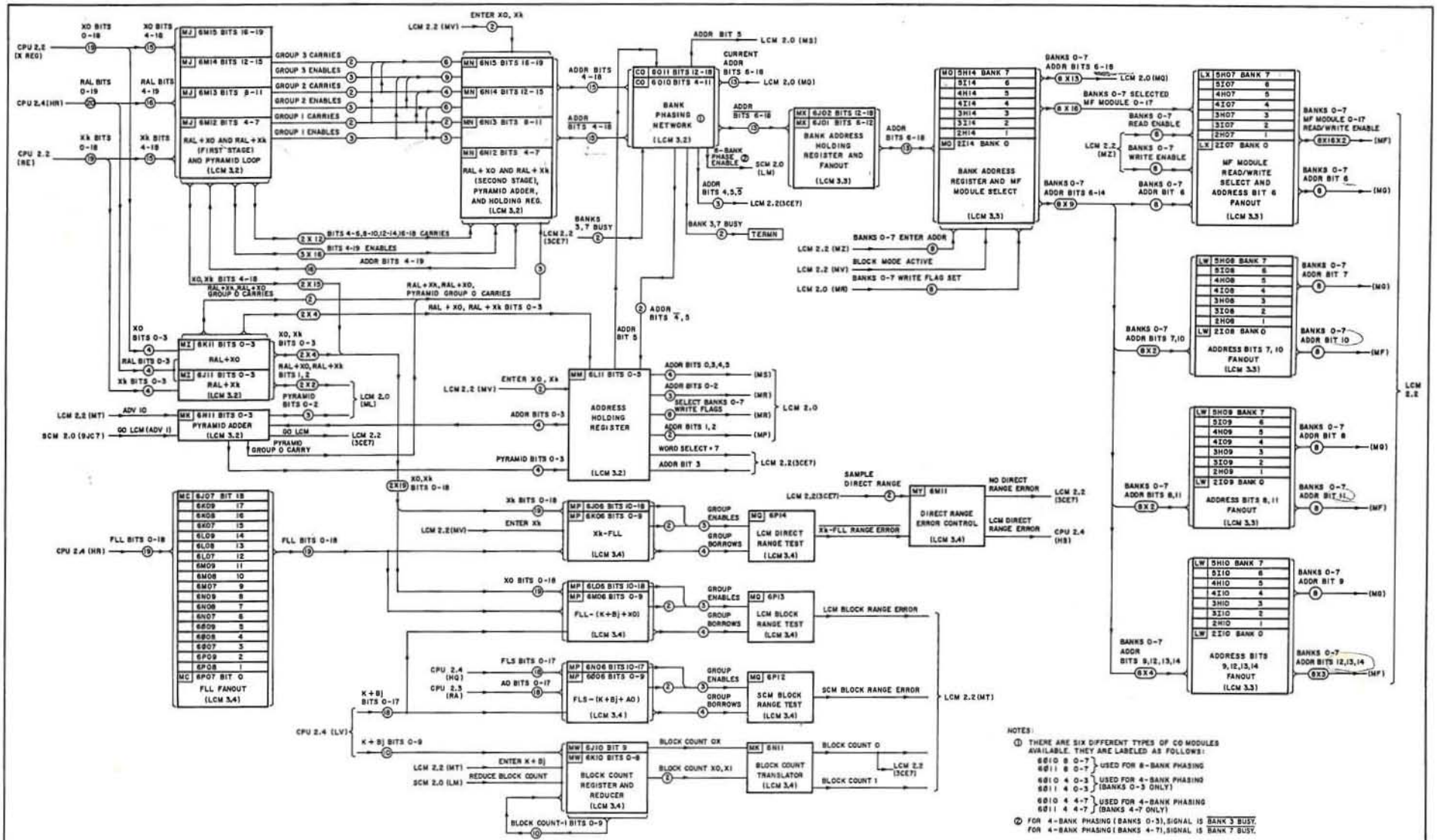
SCM BLOCK RANGE TEST

At the beginning of an LCM to SCM or SCM to LCM Block Copy (011 or 012) instruction, a test is made to ensure that all requested addresses are in the assigned SCM field. The sum of K + (Bj) is added to (A0). The resultant sum is compared with (FLS). If greater than (FLS), indicating that the block copy will exceed the assigned SCM field, the SCM Block Range Condition Flag will be set in the PSD Register and the instruction will not be executed.

Bits 0-18 from the A0 Register (RA modules), the K + Bj Adder (LV modules), and the FLS Register (HQ modules) enter the FLS - (K + Bj + A0) circuit (MP modules) directly. This circuit generates Group Enables and Group Borrows which are sent to the SCM Block Range Test circuit (MQ module). When this circuit detects an error, the PSD Register receives a SCM Block Range Error signal via the Block Control (MT module).

BLOCK COUNT CHECK

At the beginning of a block copy (011 or 012) instruction, the lowest order ten bits from the K + Bj Adder (LV modules) are gated into the Block Count Register (MW modules). The Block Control (MT module) sends the Enter K + Bj gating signal. During each subsequent clock period, the block count is decremented by one. The decreased block count is gated into the register by a Reduce Block Count signal from the SCM Access Control (LM module). A Block Count Check circuit (MW and MK modules) continually monitors the register. When the octal value is reduced to one, a Block Count 1 signal is sent to the Block Control (MT module). When it is reduced to zero, a Block Count 0 signal is sent to the Block Control and Bank Select (3CE7 modules). If the original block count was zero, the instruction will not be executed.


RAL + XO AND RAL + Xk (FIRST STAGE) AND PYRAMID LOOP (LCM 3.2)
RAL + XO AND RAL + Xk (SECOND STAGE), PYRAMID ADDER, AND HOLDING REG. (LCM 3.2)
BANK PHASING NETWORK (LCM 3.2)
BANK ADDRESS HOLDING REGISTER AND FANOUT (LCM 3.3)
BANK ADDRESS REGISTER AND MF MODULE SELECT (LCM 3.3)
MF MODULE READ/WRITE SELECT AND ADDRESS BIT 6 FANOUT (LCM 3.3)
ADDRESS BITS 7, 10 FANOUT (LCM 3.3)
ADDRESS BITS 8, 11 FANOUT (LCM 3.3)
ADDRESS BITS 9, 12, 13, 14 FANOUT (LCM 3.3)
RAL+XO
RAL+Xk (LCM 3.2)
PYRAMID ADDER (LCM 3.2)
ADDRESS HOLDING REGISTER (LCM 3.2)
FLL FANOUT (LCM 3.4)
Xk-FLL (LCM 3.4)
FLL- (K+B)+XO (LCM 3.4)
FLS-(K+B)+AO (LCM 3.4)
BLOCK COUNT REGISTER AND REDUCER (LCM 3.4)
BLOCK COUNT TRANSLATOR (LCM 3.4)
DIRECT RANGE ERROR CONTROL (LCM 3.4)
LCM DIRECT RANGE TEST (LCM 3.4)
LCM BLOCK RANGE TEST (LCM 3.4)
SCM BLOCK RANGE TEST (LCM 3.4)
NOTES:
① THERE ARE SIX DIFFERENT TYPES OF CO MODULES AVAILABLE. THEY ARE LABELED AS FOLLOWS:
② FOR 4-BANK PHASING (BANKS 0-3), SIGNAL IS BANK 3 BUSY.
FOR 4-BANK PHASING (BANKS 4-7), SIGNAL IS BANK 7 BUSY.
CONTROL DATA DEVELOPMENT DIVISION
SECONDARY BLOCK DIAGRAM ADDRESS DISTRIBUTION
60297600 AC
LCM 2.1 5-267

BANK SELECT AND SEQUENCE CONTROL

Control circuits in the 3CE7 modules select an LCM Bank and determine when a read/write cycle is to begin. Address Bits 3-5 are used to select the bank. A bank begins a read/write cycle when the Bank Select Translator (3CE7 modules) sends a Go Bank signal to one of the MZ modules. Each of these MZ modules controls the sequence of events for the corresponding LCM Bank.

BLOCK CONTROL

The Block Control Translator (MT module) generates signals which control LCM activity during block copy instructions. This module translates input signals received from the CPU, SCM, and LCM.

MEMORY STACKS

Each Bank Memory Stack contains 16 layers of vertically stacked planes. There are 512 word groups (eight 64-bit words) stored in each plane. A word group consists of a read/write drive line strung thru 512 cores. Read/write current entering the stack is applied to 16 of these drive lines on a single plane. However, a diode network diverts the current thru only one of the 16 drive lines. A sense/inhibit line also passes thru the cores. There are 512 of these lines. Each line passes thru the same core (bit) of each word group in the stack. Therefore, a single sense/inhibit line passes thru 8,192 cores.

STACK ADDRESS

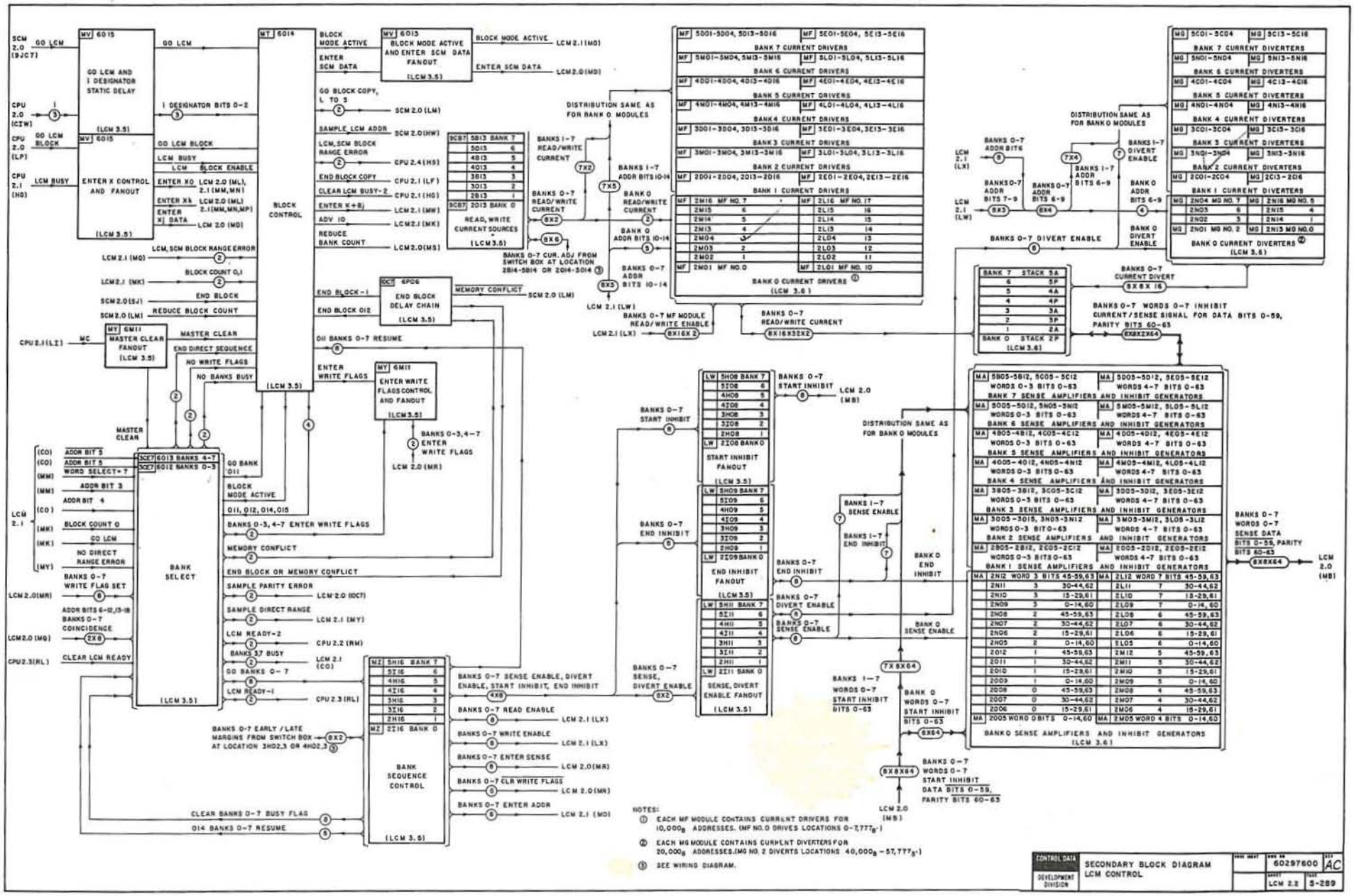
Address Bits 6-18 determine which word group (drive line) is selected for a stack reference. Bits 15-18 select one of 16 MF modules to apply read/write current to a section of the stack. The selection is indicated by the MF Module Read Enable and MF Module Write Enable signals from an LX module. Bits 10-14 select one of 32 Bank Current Drivers (MF module) to apply read/write current to 16 drive lines in the stack. Bits 6-9 select one of 16 Bank Current Diverters in each of the MG modules. Each divert circuit is connected to two drive lines on all 16 planes. The divert circuit allows current to flow thru the correct read/write drive line.

READ/SENSE

During the read portion of a bank read/write cycle, one Bank Current Driver (MF module) and eight Bank Current Diverters (MG modules) are enabled. (Only one diverter circuit is actually involved.) This allows read current to flow thru one drive line. All cores (bits) in the word group that are in a one state change to zeros. This change in state causes a signal to be transmitted thru the sense/inhibit lines to the Sense Amplifiers (MA modules). All cores that are in a zero state do not change. Therefore, no sense signal is generated. The Sense amplifiers output complemented sense data to the Bank Operand Register (MB modules). This data is gated by a Bank Sense Enable signal from the Bank Sequence Control (via LW module). After a word group has been read from a stack, all cores in that location are in a zero state. However, the word group is restored during the write portion of the bank read/write cycle with the original data or new write data.

WRITE/INHIBIT

During the write portion of the cycle, current flows thru the read/write drive line in the opposite direction. Unless this current is unopposed, all cores in the word group change to a one state. Where a zero state is required, inhibit current is passed thru the appropriate sense/inhibit line. This current opposes the write current. The resultant current is not sufficient to switch the core to a one state. Inhibit data is held in the Bank Operand Registers (MB modules). This data is the complement of write data and enables Bank Inhibit Generators (MA modules) to supply current to the sense/inhibit lines. The inhibit current flows until a Bank End Inhibit signal is generated by the Bank Sequence Control (via LW module).


SECONDARY BLOCK DIAGRAM
LCM CONTROL
60297600
AC
LCM 2.2
5-289
CONTROL DATA
DEVELOPMENT DIVISION
MV 6015
GO LCM AND I DESIGNATOR STATIC DELAY
(LCM 3.5)
MV 6015
ENTER X CONTROL AND FANOUT
(LCM 3.5)
MT 6014
BLOCK CONTROL
(LCM 3.5)
MV 6013
BLOCK MODE ACTIVE AND ENTER SCM DATA FANOUT
(LCM 3.5)
MY 6011
MASTER CLEAR FANOUT
(LCM 3.5)
MY 6011
ENTER WRITE FLAGS CONTROL AND FANOUT
(LCM 3.5)
6CT 6P06
END BLOCK DELAY CHAIN
(LCM 3.5)
BANK SELECT
(LCM 3.5)
BANK SEQUENCE CONTROL
(LCM 3.5)
READ, WRITE CURRENT SOURCES
(LCM 3.5)
BANK 0 CURRENT DRIVERS ①
(LCM 3.6)
BANK 0 CURRENT DIVERTERS ②
(LCM 3.6)
BANK 0 SENSE AMPLIFIERS AND INHIBIT GENERATORS
(LCM 3.6)
BANK 0 STACK 2P
(LCM 3.6)
BANK 0 SENSE, DIVERT ENABLE FANOUT
(LCM 3.5)
BANK 0 START INHIBIT FANOUT
(LCM 3.5)
BANK 0 END INHIBIT FANOUT
(LCM 3.5)
NOTES:
① EACH MF MODULE CONTAINS CURRENT DRIVERS FOR 10,000₈ ADDRESSES. (MF NO.0 DRIVES LOCATIONS 0-7,777₈.)
② EACH MG MODULE CONTAINS CURRENT DIVERTERS FOR 20,000₈ ADDRESSES.(MG NO. 2 DIVERTS LOCATIONS 40,000₈ - 57,777₈.)
③ SEE WIRING DIAGRAM.

Each LCM Bank contains a 480-bit (plus parity) Bank Operand Register which is located in MB modules. Each Bank Operand Register is divided into eight sections (words 0-7) of 64 bits each (60 data bits plus 4 parity bits). This register holds data in a complemented form which leaves and enters a Bank Memory Stack during a bank read/write cycle. Before entering this register, write data passes thru Storage Register A (MD modules) and Storage Register B (MC and 1DC7 modules).

SENSE/READ DATA PATH

Eight 60-bit (plus parity) data words are sensed simultaneously from a Bank Memory Stack during the read portion of the bank read/write cycle. These sense signals are amplified and complemented in the MA modules. The resultant data enters the appropriate Bank Operand Register (MB modules). Each of these modules contain four bits of the register for words 0, 2, 4, and 6 or for words 1, 3, 5, and 7. One odd word and one even word of read data are complemented and output simultaneously from all eight Bank Operand Registers to a data select and fan-in network (ME and 1DC7 modules).

SENSE/READ DATA CONTROL

Sense data entering a Bank Operand Register is under the control of logic circuits and flags contained within the MR modules. Words 0-7 Sense Flags must all be set and Words 0-7 Write Flags must all be clear before all word sections of the register can be entered with sense data. The Sense Flags are all set when the Bank Sequence Control (MZ module) generates a Clear Write Flags signal. When the MZ module generates a Enter Sense signal, sense data is allowed to enter the word sections of the Bank Operand Register in which the corresponding Sense Flags are set and Write Flags are clear.

Read data leaving a Bank Operand Register is under the control of Odd and Even Bank Address Bits 1 and 2. These address bits are held in a register located in the ML modules. These modules also contain circuits which select the proper address source. RAL + Xk is selected for direct references; RAL + X0 is selected for the first word in a block copy; the pyramid is selected for all subsequent words in a block copy. When Pyramid Bit 0 is set and pyramid address has been selected, only odd Bank Operand Registers will receive address bits 1 and 2. When Pyramid Bit 0 is clear and pyramid address has been selected, only even registers will receive address bits 1 and 2. A word select translator for these address bits is located in each MB module.

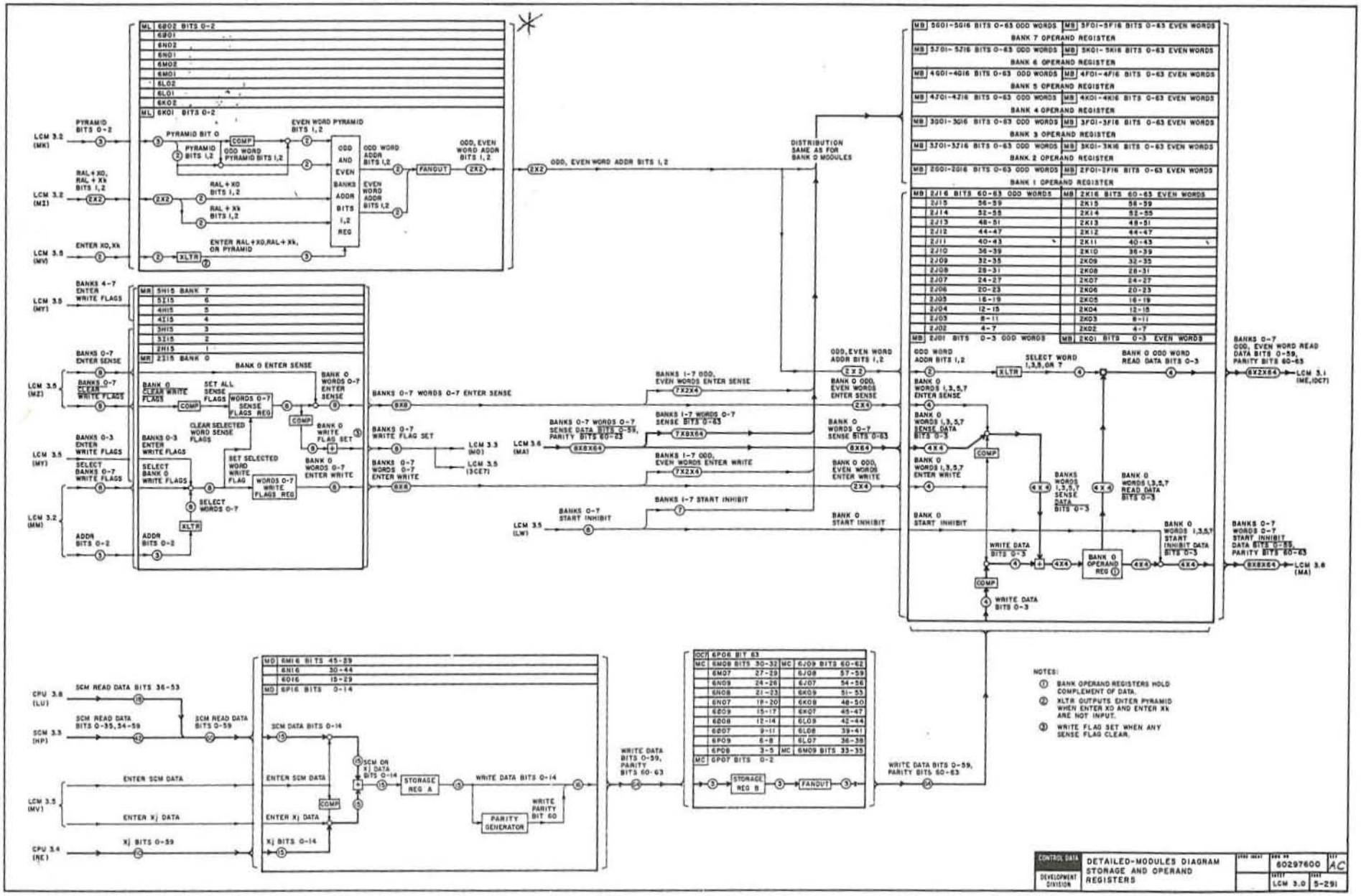
WRITE/INHIBIT DATA PATH

Data which is to be written into a Bank Memory Stack originates at either an X Register or the SRO Register in SCM. The selected 60-bit word first enters Storage Register A (MD modules). One parity bit is formed for each 15-bit section of the 60-bit word in this register. In the following clock period, the 64 bits of data and parity are transferred to Storage Register B (MC and 1DC7 modules). This data (plus parity) is fanned-out in the following clock period to all eight Bank Operand Registers (MB modules). The data (plus parity) enters a selected register in a complemented form. Data enters the selected register one 60-bit (plus parity) word at a time. When data enters a word section of the Bank Operand Register, the corresponding word Sense Flag is cleared. This prevents entering sense data over the write data during the bank read cycle. This data is used during the write portion of a bank read/write cycle to activate Bank Inhibit Generators (MA modules). All 480 bits (plus parity) of inhibit data are transmitted to the MA modules simultaneously.

WRITE/INHIBIT DATA CONTROL

Write data entering Storage Register A is selected by Enter SCM Data and Enter Xj Data signals which are generated by the MV module. The data passes thru Storage Registers A and B in successive clock periods with no control signals required. Write data entering a Bank Operand Register is under control of Words 0-7 Write Flags (MR modules) which are individually set for one clock period. These flags are set by Address Bits 0-2 (word select) and Enter Write Flags and Select Bank Write Flags control signals (bank select). The corresponding word Sense Flag is cleared at this time. Inhibit data leaving a Bank Operand Register is under control of a Start Inhibit signal generated by the Bank Sequence Control.

130


ML 6R02 BITS 0-2
6R01
6N02
6N01
6M02
6M01
6L02
6L01
6K02
ML 6K01 BITS 0-2
LCM 3.2 (MX)
PYRAMID BITS 0-2
PYRAMID BIT 0
COMP
PYRAMID BITS 1,2
ODD WORD PYRAMID BITS 1,2
EVEN WORD PYRAMID BITS 1,2
ODD AND EVEN BANKS ADDR BITS 1,2 REG
ODD WORD ADDR BITS 1,2
EVEN WORD ADDR BITS 1,2
FANOUT
ODD, EVEN WORD ADDR BITS 1,2
LCM 3.2 (MZ)
RAL+XO, RAL+Xk BITS 1,2
RAL+XO BITS 1,2
RAL+Xk BITS 1,2
LCM 3.5 (MV)
ENTER XO, Xk
ENTER RAL+XO, RAL+Xk, OR PYRAMID
XLTR
DISTRIBUTION SAME AS FOR BANK 0 MODULES
MB 5G01-5G16 BITS 0-63 ODD WORDS
MB 5F01-5F16 BITS 0-63 EVEN WORDS
BANK 7 OPERAND REGISTER
MB 5J01-5J16 BITS 0-63 ODD WORDS
MB 5K01-5K16 BITS 0-63 EVEN WORDS
BANK 6 OPERAND REGISTER
MB 4G01-4G16 BITS 0-63 ODD WORDS
MB 4F01-4F16 BITS 0-63 EVEN WORDS
BANK 5 OPERAND REGISTER
MB 4J01-4J16 BITS 0-63 ODD WORDS
MB 4K01-4K16 BITS 0-63 EVEN WORDS
BANK 4 OPERAND REGISTER
MB 3G01-3G16 BITS 0-63 ODD WORDS
MB 3F01-3F16 BITS 0-63 EVEN WORDS
BANK 3 OPERAND REGISTER
MB 3J01-3J16 BITS 0-63 ODD WORDS
MB 3K01-3K16 BITS 0-63 EVEN WORDS
BANK 2 OPERAND REGISTER
MB 2G01-2G16 BITS 0-63 ODD WORDS
MB 2F01-2F16 BITS 0-63 EVEN WORDS
BANK 1 OPERAND REGISTER
MB 2J16 BITS 60-63 ODD WORDS
MB 2K16 BITS 60-63 EVEN WORDS
2J15 56-59
2K15 56-59
2J14 52-55
2K14 52-55
2J13 48-51
2K13 48-51
2J12 44-47
2K12 44-47
2J11 40-43
2K11 40-43
2J10 36-39
2K10 36-39
2J09 32-35
2K09 32-35
2J08 28-31
2K08 28-31
2J07 24-27
2K07 24-27
2J06 20-23
2K06 20-23
2J05 16-19
2K05 16-19
2J04 12-15
2K04 12-15
2J03 8-11
2K03 8-11
2J02 4-7
2K02 4-7
MB 2J01 BITS 0-3 ODD WORDS
MB 2K01 BITS 0-3 EVEN WORDS
ODD WORD ADDR BITS 1,2
SELECT WORD 1,3,5,OR 7
BANK 0 ODD WORD READ DATA BITS 0-3
BANKS 0-7 ODD, EVEN WORD READ DATA BITS 0-59, PARITY BITS 60-63
8X2X64
LCM 3.1 (ME,10C7)
LCM 3.5 (MY)
BANKS 4-7 ENTER WRITE FLAGS
MR 5H15 BANK 7
5J15 6
4H15 5
4J15 4
3H15 3
3J15 2
2H15 1
MR 2J15 BANK 0
BANK 0 ENTER SENSE
BANKS 0-7 ENTER SENSE
BANK 0 CLEAR WRITE FLAGS
BANKS 0-7 CLEAR WRITE FLAGS
SET ALL SENSE FLAGS
WORDS 0-7 SENSE FLAGS REG
BANK 0 WORDS 0-7 ENTER SENSE
BANKS 0-7 WORDS 0-7 ENTER SENSE
8X8
BANKS 0-7 WRITE FLAG SET
BANK 0 WRITE FLAG SET
CLEAR SELECTED WORD SENSE FLAGS
BANKS 0-3 ENTER WRITE FLAGS
SELECT BANKS 0-7 WRITE FLAGS
SET SELECTED WORD WRITE FLAG
WORDS 0-7 WRITE FLAGS REG
SELECT BANK 0 WRITE FLAGS
SELECT WORDS 0-7
BANK 0 WORDS 0-7 ENTER WRITE
BANKS 0-7 WORDS 0-7 ENTER WRITE
8X4
LCM 3.3 (MO)
LCM 3.5 (3CE7)
LCM 3.2 (MM)
ADDR BITS 0-2
BANKS 1-7 ODD, EVEN WORDS ENTER SENSE
7X2X4
BANKS 1-7 WORDS 0-7 SENSE BITS 0-63
7X8X64
BANKS 0-7 WORDS 0-7 SENSE DATA BITS 0-59, PARITY BITS 60-63
8X8X64
LCM 3.6 (MA)
BANKS 1-7 ODD, EVEN WORDS ENTER WRITE
BANKS 1-7 START INHIBIT
BANKS 0-7 START INHIBIT
LCM 3.5 (LW)
ODD, EVEN WORD ADDR BITS 1,2
BANK 0 ODD, EVEN WORDS ENTER SENSE
2X4
BANK 0 WORDS 0-7 SENSE BITS 0-63
8X64
BANK 0 ODD, EVEN WORDS ENTER WRITE
BANK 0 START INHIBIT
BANK 0 WORDS 1,3,5,7 ENTER SENSE
BANK 0 WORDS 1,3,5,7 SENSE DATA BITS 0-3
4X4
BANK 0 WORDS 1,3,5,7 ENTER WRITE
BANKS WORDS 1,3,5,7 SENSE DATA BITS 0-3
BANK 0 WORDS 1,3,5,7 READ DATA BITS 0-3
BANK 0 WORDS 1,3,5,7 START INHIBIT DATA BITS 0-3
WRITE DATA BITS 0-3
BANK 0 OPERAND REG (1)
BANKS 0-7 WORDS 0-7 START INHIBIT DATA BITS 0-59, PARITY BITS 60-63
8X8X64
LCM 3.8 (MA)
CPU 3.8 (LU)
SCM READ DATA BITS 36-53
SCM 3.3 (HP)
SCM READ DATA BITS 0-35, 54-59
SCM READ DATA BITS 0-59
MD 6M16 BITS 45-59
6N16 30-44
6O16 15-29
MD 6P16 BITS 0-14
SCM DATA BITS 0-14
LCM 3.5 (MV)
ENTER SCM DATA
ENTER Xj DATA
SCM OR Xj DATA BITS 0-14
STORAGE REG A
WRITE DATA BITS 0-14
PARITY GENERATOR
WRITE PARITY BIT 60
CPU 3.4 (NE)
Xj BITS 0-59
Xj BITS 0-14
WRITE DATA BITS 0-59, PARITY BITS 60-63
OCT 6P06 BIT 63
MC 6M08 BITS 30-32
MC 6J09 BITS 60-62
6M07 27-29
6J08 57-59
6N09 24-26
6J07 54-56
6N08 21-23
6K09 51-53
6N07 18-20
6K08 48-50
6O09 15-17
6K07 45-47
6O08 12-14
6L09 42-44
6O07 9-11
6L08 39-41
6P09 6-8
6L07 36-38
6P08 3-5
MC 6M09 BITS 33-35
MC 6P07 BITS 0-2
STORAGE REG B
FANOUT
WRITE DATA BITS 0-59, PARITY BITS 60-63
NOTES:
① BANK OPERAND REGISTERS HOLD COMPLEMENT OF DATA.
② XLTR OUTPUTS ENTER PYRAMID WHEN ENTER XO AND ENTER Xk ARE NOT INPUT.
③ WRITE FLAG SET WHEN ANY SENSE FLAG CLEAR.
CONTROL DATA DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM STORAGE AND OPERAND REGISTERS
60297600 AC
LCM 3.0 5-291

STORAGE READOUT DATA PATH

Odd and even word read data from the Bank Operand Registers (MB modules) is merged in a data select and fan-in network (ME and 1DC7 modules). The selected 60-bit (plus parity) word is entered into the Read Register (MC modules). This word (less parity) is also sent to an X Register. Data in the Read Register is sent to SWF in SCM during the following clock period.

STORAGE READOUT DATA CONTROL

Selection of the storage readout word is determined by address bits 0, 3, 4, and 5 from the MS modules. When the Reduce Bank Count signal from the MT module is present, the octal value of bits 3-5 will be reduced by two. Data leaving LCM is dependent on gating signals at the destination registers.

PARITY CHECK

The MC, MI, and MS modules contain circuits that check the four 15-bit sections of the word for errors that may have occurred during an LCM bank reference. An odd number of ones (odd parity) should exist in each section including the corresponding parity bit. All four sections of the word are checked in the same manner. The four results are entered into the LCM Parity Error Register (HT module). This register is monitored by the MCU.

Each MC module contains three bits of the Read Register and a Group Parity Check circuit. This circuit checks the condition of the three-bit group in the register. If an odd number of ones exist, the Group Parity Check Bit will be a one. These 20 bits are sent to four Section Parity Check circuits in the MI or MS modules. These circuits each check five Group Parity Check Bits. A Section 0 Parity Error will be sent to the LCM Parity Error Register (HT module) when the following conditions exist: Groups 0-4 Parity Check Bits consist of an odd number of ones and Read Parity Bit 60 is a one, or Groups 0-4 Parity Check Bits consist of an even number of ones and Read Parity Bit 60 is a zero. Sections 1-3 are handled in the same manner.

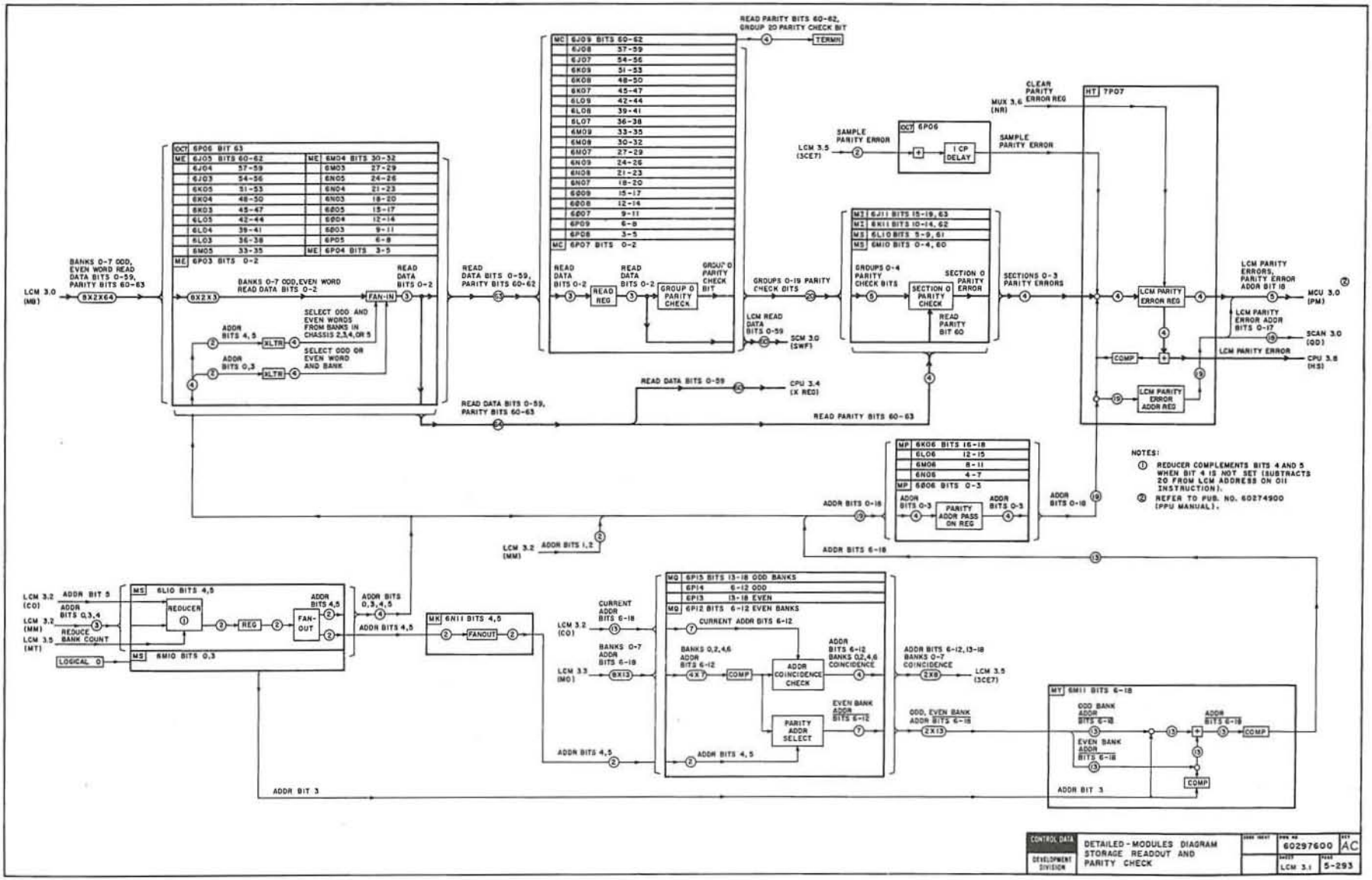
PARITY ERROR ADDRESS

The HT module also contains a LCM Parity Error Address Register. This register holds the LCM address at which a parity error has occurred. LCM addresses are entered into this register every clock period if none of the LCM Parity Error Register bits are ones. When a parity error does occur, one or more of these bits will be a one. This blocks entry of any subsequent addresses in the LCM Parity Error Address Register. Address Bits 6-18 enter the register from a Bank Address Register (MO module) via MQ, MY, and MP modules. Address Bits 0, 3, 4, and 5 enter the register from the Address Holding Register (MM module) via MS and MP modules. Address Bits 1 and 2 enter the register from the Address Holding Register via an MP module. The selection of Address Bits 6-18 is dependent on the condition of Address Bits 3-5. These bits determine which Bank Address Register contains the parity error address.

ADDRESS COINCIDENCE CHECK

The MQ modules contain an Address Coincidence Check circuit. This circuit determines if a word stored in a Bank Memory Stack is also contained in the corresponding Bank Operand Register (MB modules) due to a previously issued instruction. A comparison is made between Current Address Bits 6-18 from the Bank Phasing Network (CO modules) and the address in each Bank Address Register (MO modules). If coincidence exists for the selected bank, a read/write cycle will not be initiated during a Read LCM to X (014) instruction. The word is transmitted directly from the Bank Operand Register to an X Register.

The LCM words required for an LCM to SCM Block Copy (011) instruction may be in one of the Bank Operand Registers. This situation is not sensed. The words in the register are discarded and reread from a Bank Memory Stack.



CONTROL DATA DEVELOPMENT DIVISION	DETAILED - MODULES DIAGRAM STORAGE READOUT AND PARITY CHECK	DOC NO. 60297600	REV AC
		MODEL LCM 3.1	PAGE 5-293

All LCM addresses are formed by the Address Adder. This two-stage adder is located within MI, MJ, MK, and MN modules. Address bits 4-18 are held in a Partial Sum Address Holding Register (MN modules). The lowest order bits are held in Address Bits 0-3 Holding Register (MM module). One of three types of addresses are entered into these registers. They are direct sequence addresses, initial block copy addresses, and subsequent block copy addresses. Address Bits 4-18 pass thru a Bank Phasing Network (CO modules) before being used in LCM control.

DIRECT SEQUENCE ADDRESS

In a Read LCM to X or Write X to LCM (014 or 015) instruction, the LCM address is formed by adding the lowest order 19 bits of the Xk Register to (RAL). The sum (or partial sum) of these operands is gated into the holding registers when Enter Xk is generated by the MV module.

BLOCK COPY ADDRESSES

INITIAL ADDRESS

In an LCM to SCM or SCM to LCM Block Copy (011 or 012) instruction, the first LCM address is formed by adding the lowest 19 bits of the X0 Register to (RAL). The sum (or partial sum) of these operands is gated into the holding registers when Enter X0 is generated by the MV module.

SUBSEQUENT ADDRESSES

All remaining addresses in a block copy are formed by the Pyramid adder (MK and MJ modules). This adder increases the initial address by 1 or 10 (octal) when a Go LCM or Advance 10 signal is present. A Go LCM signal indicates that an SCM address has been accepted in the SAS. This allows the next sequential LCM word to be referenced. An Advance 10 signal will be present during an LCM to SCM Block Copy instruction only. This allows the next sequential LCM Bank to be referenced.

BANK PHASING NETWORKS

There are three different Bank Phasing Networks. Each type requires a different set of CO modules.

EIGHT-BANK PHASING

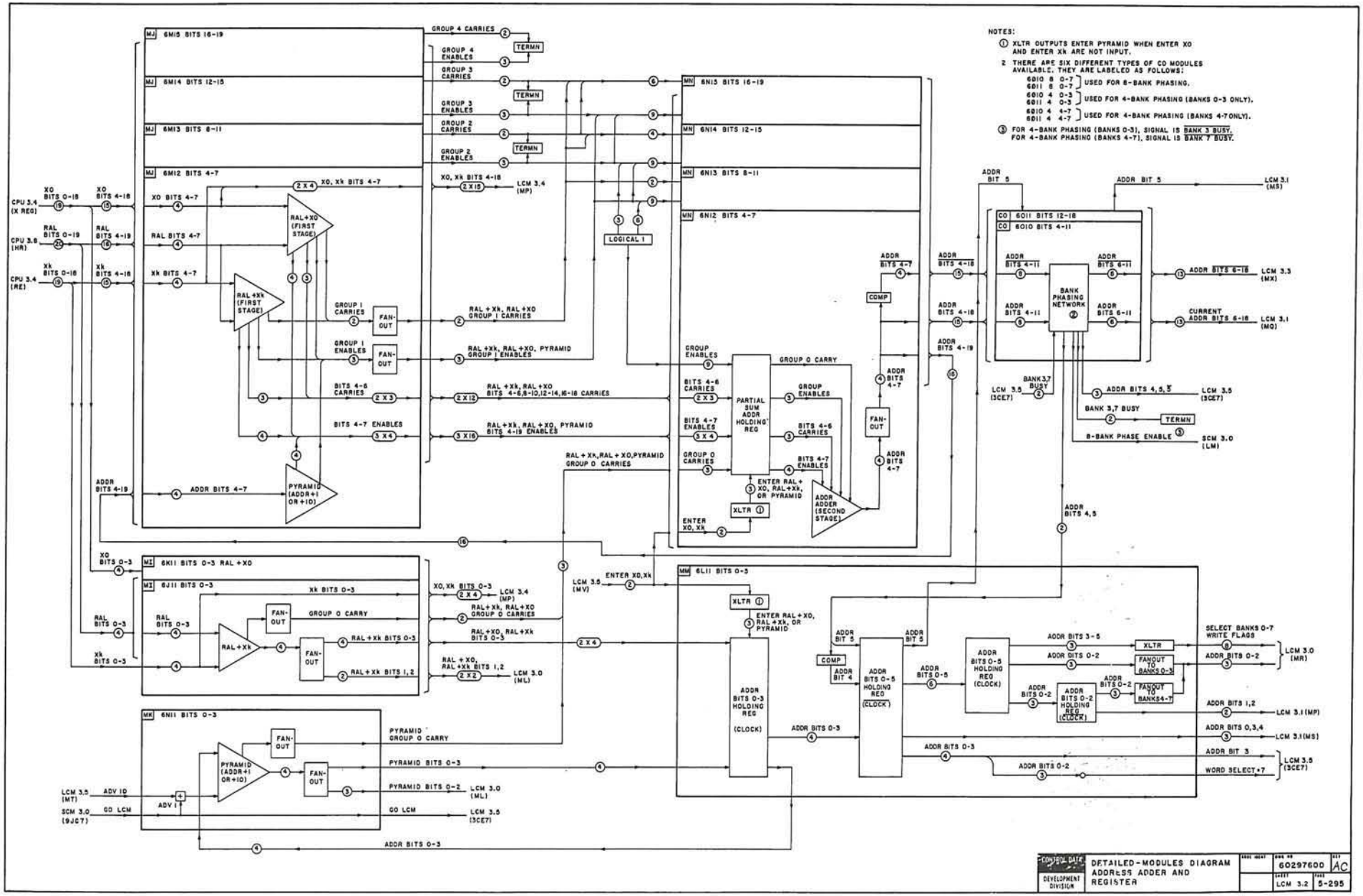
When all eight LCM Banks are used, Address Bits 4-18 pass thru the network unchanged. The Banks 3 and 7 Busy signals from the Bank Select (3CE7 modules) are terminated. An 8-Bank Phase Enable signal is sent to the SCM Access Control (LM module).

FOUR-BANK PHASING (BANKS 0-3)

When LCM Ranks 0-3 only are used, Address Bit 4 passes thru unchanged, Address Bit 5 is forced to zero, Address Bits 6-17 are shifted one bit position to the left, bit 18 is terminated. The Bank 3 Busy signal from the Bank Select (3CE7 module) is complemented and sent to the SCM Access Control (LM module). The Bank 7 Busy signal is terminated.

FOUR-BANK PHASING (BANKS 4-7)

When LCM Banks 4-7 only are used, Address Bit 4 passes thru unchanged, Address Bit 5 is forced to one, Address Bits 6-17 are shifted one bit position to the left; bit 18 is terminated. The Bank 7 Busy signal from the Bank Select (3CE7 module) is complemented and sent to the SCM Access Control (LM module). The Bank 3 Busy signal is terminated.


NOTES:
1. XLTR OUTPUTS ENTER PYRAMID WHEN ENTER XO AND ENTER Xk ARE NOT INPUT.
2. THERE ARE SIX DIFFERENT TYPES OF CO MODULES AVAILABLE. THEY ARE LABELED AS FOLLOWS:
6010 8 0-7, 6011 8 0-7 USED FOR 8-BANK PHASING.
6010 4 0-3, 6011 4 0-3 USED FOR 4-BANK PHASING (BANKS 0-3 ONLY).
6010 4 4-7, 6011 4 4-7 USED FOR 4-BANK PHASING (BANKS 4-7 ONLY).
3. FOR 4-BANK PHASING (BANKS 0-3), SIGNAL IS BANK 3 BUSY. FOR 4-BANK PHASING (BANKS 4-7), SIGNAL IS BANK 7 BUSY.
6M15 BITS 16-19
6M14 BITS 12-15
6M13 BITS 8-11
6M12 BITS 4-7
6N15 BITS 16-19
6N14 BITS 12-15
6N13 BITS 8-11
6N12 BITS 4-7
6K11 BITS 0-3 RAL +XO
6J11 BITS 0-3
6N11 BITS 0-3
6L11 BITS 0-3
CO 6011 BITS 12-18
CO 6010 BITS 4-11
GROUP 4 CARRIES
GROUP 4 ENABLES
GROUP 3 CARRIES
GROUP 3 ENABLES
GROUP 2 CARRIES
GROUP 2 ENABLES
TERMN
LOGICAL 1
XO BITS 0-18
XO BITS 4-18
RAL BITS 0-19
RAL BITS 4-19
Xk BITS 0-18
Xk BITS 4-18
CPU 3.4 (X REG)
CPU 3.8 (MR)
CPU 3.4 (ME)
XO BITS 4-7
RAL BITS 4-7
Xk BITS 4-7
RAL+XO (FIRST STAGE)
RAL+Xk (FIRST STAGE)
PYRAMID (ADDR+1 OR +10)
XO, Xk BITS 4-7
XO, Xk BITS 4-18
LCM 3.4 (MP)
GROUP 1 CARRIES
GROUP 1 ENABLES
FAN-OUT
RAL + Xk, RAL + XO GROUP 1 CARRIES
RAL +Xk, RAL +XO, PYRAMID GROUP 1 ENABLES
BITS 4-6 CARRIES
BITS 4-7 ENABLES
RAL + Xk, RAL + XO BITS 4-6,8-10,12-14,16-18 CARRIES
RAL +Xk, RAL + XO, PYRAMID BITS 4-19 ENABLES
ADDR BITS 4-19
ADDR BITS 4-7
RAL + Xk, RAL + XO, PYRAMID GROUP 0 CARRIES
GROUP ENABLES
BITS 4-6 CARRIES
BITS 4-7 ENABLES
GROUP 0 CARRIES
PARTIAL SUM ADDR HOLDING REG
GROUP 0 CARRY
ENTER RAL + XO, RAL+Xk, OR PYRAMID
XLTR 1
ENTER XO, Xk
ADDR ADDER (SECOND STAGE)
COMP
ADDR BIT 4
ADDR BIT 5
ADDR BITS 4-18
ADDR BITS 4-19
ADDR BITS 4-11
ADDR BITS 6-11
BANK PHASING NETWORK 2
ADDR BITS 6-18
CURRENT ADDR BITS 6-18
LCM 3.1 (MS)
LCM 3.3 (MX)
LCM 3.1 (MQ)
BANK 3,7 BUSY
LCM 3.5 (3CE7)
ADDR BITS 4,5,5
8-BANK PHASE ENABLE 3
SCM 3.0 (LM)
ADDR BITS 4,5
XO BITS 0-3
RAL BITS 0-3
Xk BITS 0-3
RAL+Xk
GROUP 0 CARRY
RAL+Xk BITS 0-3
RAL+Xk BITS 1,2
XO, Xk BITS 0-3
RAL+Xk, RAL+XO GROUP 0 CARRIES
RAL+XO, RAL+Xk BITS 0-3
RAL + XO, RAL+Xk BITS 1,2
LCM 3.0 (ML)
LCM 3.5 (MV)
ENTER XO,Xk
ADDR BITS 0-3 HOLDING REG (CLOCK)
ADDR BITS 0-5
ADDR BITS 0-5 HOLDING REG (CLOCK)
ADDR BITS 0-2 HOLDING REG (CLOCK)
ADDR BITS 3-5
ADDR BITS 0-2
XLTR
FANOUT TO BANKS 0-3
FANOUT TO BANKS4-7
SELECT BANKS 0-7 WRITE FLAGS
LCM 3.0 (MR)
ADDR BITS 1,2
LCM 3.1 (MP)
ADDR BITS 0,3,4
LCM 3.1 (MS)
ADDR BIT 3
WORD SELECT *7
LCM 3.5 (3CE7)
PYRAMID GROUP 0 CARRY
PYRAMID BITS 0-3
PYRAMID BITS 0-2
LCM 3.0 (ML)
GO LCM
LCM 3.5 (3CE7)
LCM 3.5 (MT)
ADV 10
ADV 1
SCM 3.0 (9JC7)
ADDR BITS 0-3
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM
ADDRESS ADDER AND REGISTER
60297600
AC
LCM 3.2
5-295

DETAILED-MODULES DIAGRAM
BANK ADDRESS REGISTERS AND FANOUTS

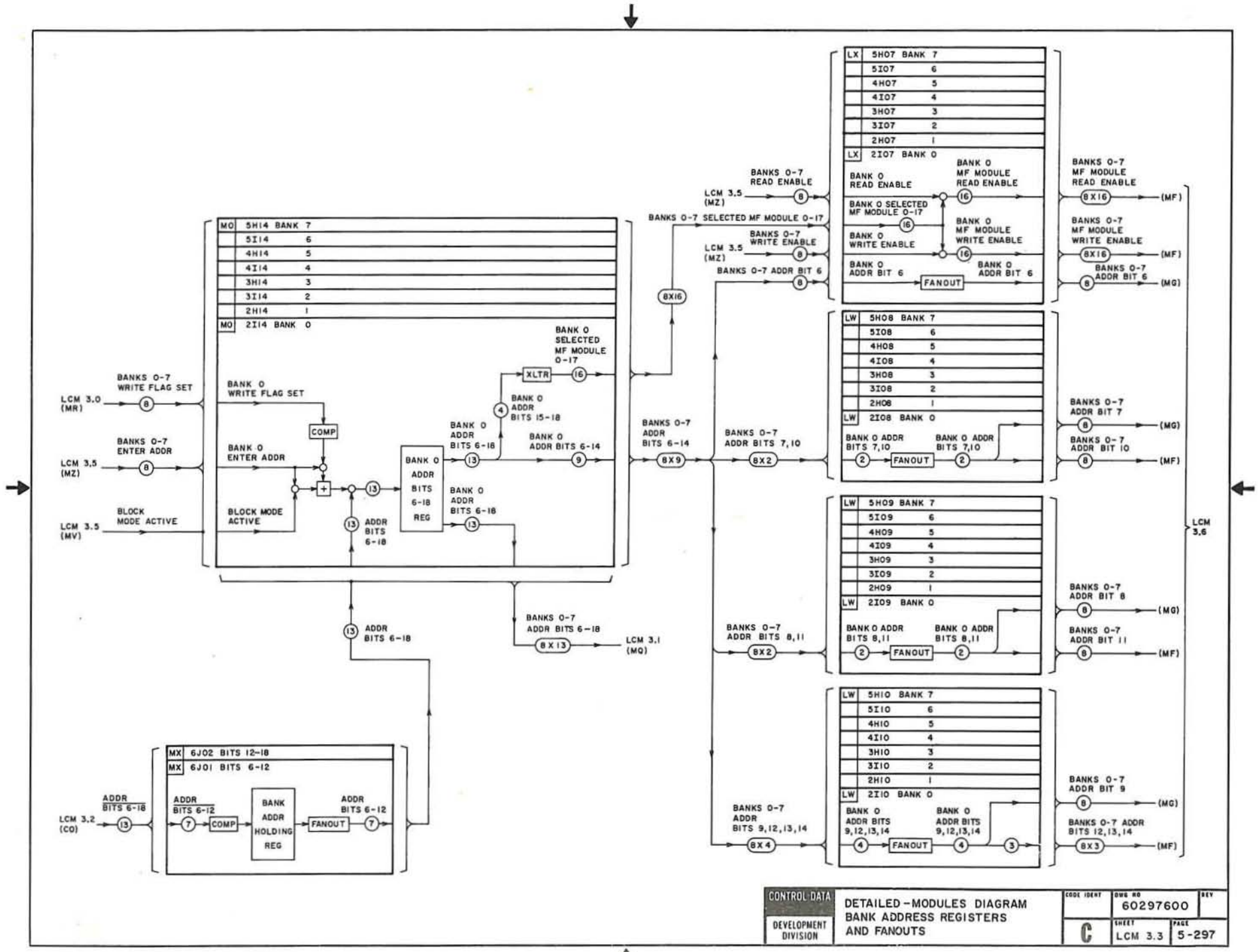
The Bank Address Holding Register is contained within MX modules. Address Bits 6-18 arrive in a complemented form from the Bank Phasing Network (CO modules). This bank address is complemented before entering the register.

The output of the Bank Address Holding Register is fanned-out to each individual Bank Address Register. Each register is contained within a MO module. An address enters a selected register when the following conditions exist: Bank X Enter Address · (Block Mode Active + $\overline{\text{Bank X Write Flag Set}}$).

Each Bank Address Register sends its output to the Address Coincidence Check circuit (MQ modules). Bits 6-9 are sent to the MG modules where they select a Current Divert circuit. Bits 10-14 are sent to the MF modules where they select a Current Driver circuit. Address Bit 6 is fanned-out in LX modules. Address Bits 7-14 are fanned-out in LW modules.

Address Bits 15-18 from the Bank Address Registers are translated in the MO modules. This translation determines which one of 16 MF modules for each bank is selected for a specific address.

The LX modules generate MF Module Read/Write Enable signals. These signals are dependent on the above translation and Read/Write signals from the selected Bank Sequence Control (MZ module).



CONTROL DATA
DEVELOPMENT DIVISION

DETAILED - MODULES DIAGRAM
BANK ADDRESS REGISTERS
AND FANOUTS

CODE IDENT C
DWG NO 60297600
REV
SHEET LCM 3.3
PAGE 5-297

LCM DIRECT RANGE TEST

During a direct read or write (014 or 015) instruction, the lowest order 19 bits of (Xk) are compared with (FLL) to determine if the requested address is in the assigned LCM field. If (Xk) is greater than or equal to (FLL), the LCM Direct Range Condition Flag will be set in the PSD Register. Also, if a direct write instruction was issued, the data will not be sent to LCM.

Bits 0-18 from the FLL Register (HR modules) pass thru a fanout (MC modules) before entering the Xk-FLL circuit (MP modules). Bits 0-18 from the Xk Register (via MI and MJ modules) are complemented and gated into Operand A Register (MP modules) before entering the test circuit. This operand is gated by Enter Xk from the MV module. The Xk-FLL circuit generates Group Enables and Group Borrows which are sent to the LCM Direct Range Test circuit (MQ module). This circuit outputs a one when Xk-FLL Range Error does not exist. This signal (No Direct Range Error) is sent to the 3CE7 modules via the MY module. When the test circuit outputs a zero, the PSD Register (HS module) receives a LCM Direct Range Error signal from the MY module. This signal is gated when either 3CE7 module generates a Sample Direct Range signal.

LCM BLOCK RANGE TEST

At the beginning of an LCM to SCM or SCM to LCM Block Copy (011 or 012) instruction, a test is made to ensure that all requested addresses are in the assigned LCM field. The sum of K + (Bj) is added to the lowest order 19 bits of (X0). The resultant sum is compared with (FLL). If greater than (FLL), indicating that the block copy will exceed the assigned LCM field, the LCM Block Range Condition Flag will be set in the PSD Register and the instruction will not be executed.

Bits 0-18 from the X0 Register enter the FLL - (K + Bj + X0) circuit (MP modules) via the MI and MJ modules. Bits 0-17 from the K + Bj Adder (LV modules) enter the test circuit directly. Bits 0-18 from the FLL Register (via MC modules) are complemented and enter Operand A Register before entering the test circuit. The FLL - (K + Bj + X0) circuit generates Group Enables and Group Borrows which are sent to the LCM Block Range Test circuit (MQ module). When this circuit outputs a one, the PSD Register receives a LCM Block Range Error signal via the Block Control (MT module).

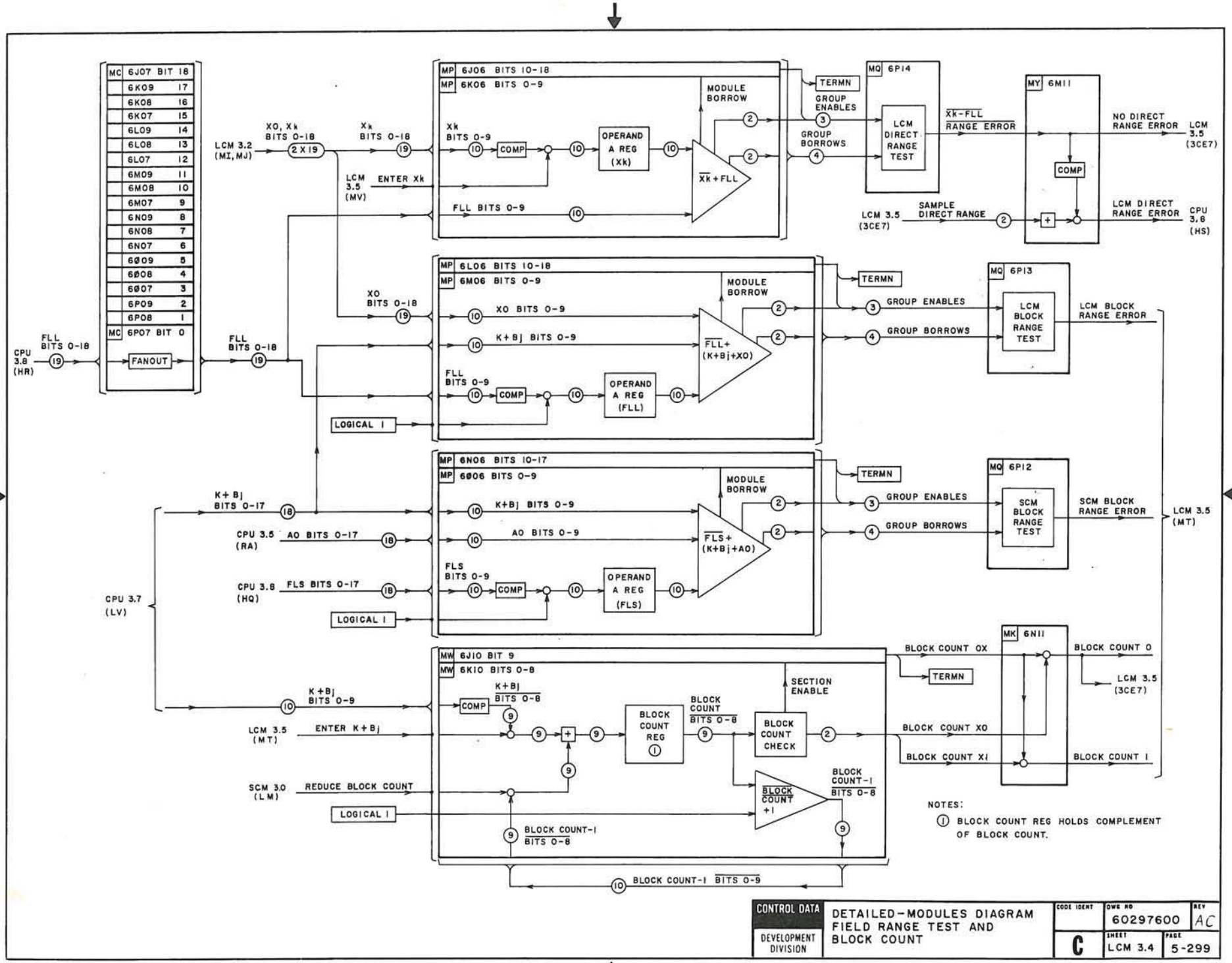
SCM BLOCK RANGE TEST

At the beginning of an LCM to SCM or SCM to LCM Block Copy (011 or 012) instruction, a test is made to ensure that all requested addresses are in the assigned SCM field. The sum of K + (Bj) is added to (A0). The resultant sum is compared with (FLS). If greater than (FLS), indicating that the block copy will exceed the assigned SCM field, the SCM Block Range Condition Flag will be set in the PSD Register and the instruction will not be executed.

Bits 0-18 from the A0 Register (RA modules) and the K + Bj Adder (LV modules) enter the FLS - (K + Bj + A0) circuit (MP modules) directly. Bits 0-18 from the FLS Register (HQ modules) are complemented and enter Operand A Register before entering the test circuit. This circuit generates Group Enables and Group Borrows which are sent to the SCM Block Range Test circuit (MQ module). When this circuit outputs a one, the PSD Register receives a SCM Block Range Error signal via the Block Control (MT module).

BLOCK COUNT CHECK

At the beginning of a block copy (011 or 012) instruction, the lowest order ten bits from the K + Bj Adder (LV modules) are gated into the Block Count Register (MW modules). The Block Control (MT module) sends the Enter K + Bj gating signal. During each subsequent clock period, the block count is decremented by one. The decreased block count is gated into the register by a Reduce Block Count signal from the SCM Access Control (LM module). A Block Count Check circuit (MW and MK modules) continually monitors the register. When the octal value is reduced to one, a Block Count 1 signal is sent to the Block Control (MT module). When it is reduced to zero, a Block Count 0 signal is sent to the Block Control and Bank Select (3CE7 modules).


MC 6J07 BIT 18
6K09 17
6K08 16
6K07 15
6L09 14
6L08 13
6L07 12
6M09 11
6M08 10
6M07 9
6N09 8
6N08 7
6N07 6
6Ø09 5
6Ø08 4
6Ø07 3
6P09 2
6P08 1
MC 6P07 BIT 0
FANOUT
CPU 3.8 (HR)
FLL BITS 0-18
LCM 3.2 (MI, MJ)
XO, Xk BITS 0-18
2 X 19
Xk BITS 0-18
LCM 3.5 (MV)
ENTER Xk
MP 6J06 BITS 10-18
MP 6K06 BITS 0-9
Xk BITS 0-9
COMP
OPERAND A REG (Xk)
FLL BITS 0-9
Xk + FLL
MODULE BORROW
TERMN
GROUP ENABLES
GROUP BORROWS
MQ 6P14
LCM DIRECT RANGE TEST
Xk-FLL RANGE ERROR
MY 6M11
NO DIRECT RANGE ERROR
LCM 3.5 (3CE7)
COMP
LCM 3.5 (3CE7)
SAMPLE DIRECT RANGE
LCM DIRECT RANGE ERROR
CPU 3.8 (HS)
MP 6L06 BITS 10-18
MP 6M06 BITS 0-9
XO BITS 0-18
XO BITS 0-9
K+Bj BITS 0-9
FLL BITS 0-9
COMP
OPERAND A REG (FLL)
FLL+ (K+Bj+XO)
LOGICAL 1
MQ 6P13
LCM BLOCK RANGE TEST
LCM BLOCK RANGE ERROR
MP 6N06 BITS 10-17
MP 6Ø06 BITS 0-9
K+Bj BITS 0-17
CPU 3.5 (RA)
AO BITS 0-17
CPU 3.8 (HQ)
FLS BITS 0-17
CPU 3.7 (LV)
AO BITS 0-9
FLS BITS 0-9
COMP
OPERAND A REG (FLS)
FLS+ (K+Bj+AO)
LOGICAL 1
MQ 6P12
SCM BLOCK RANGE TEST
SCM BLOCK RANGE ERROR
LCM 3.5 (MT)
MW 6J10 BIT 9
MW 6K10 BITS 0-8
K+Bj BITS 0-9
K+Bj BITS 0-8
COMP
LCM 3.5 (MT)
ENTER K+Bj
SCM 3.0 (LM)
REDUCE BLOCK COUNT
LOGICAL 1
BLOCK COUNT REG (1)
BLOCK COUNT BITS 0-8
SECTION ENABLE
BLOCK COUNT CHECK
BLOCK COUNT+1
BLOCK COUNT-1 BITS 0-8
BLOCK COUNT-1 BITS 0-8
BLOCK COUNT-1 BITS 0-9
BLOCK COUNT OX
TERMN
BLOCK COUNT XO
BLOCK COUNT XI
MK 6N11
BLOCK COUNT 0
LCM 3.5 (3CE7)
BLOCK COUNT 1
NOTES:
(1) BLOCK COUNT REG HOLDS COMPLEMENT OF BLOCK COUNT.
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM
FIELD RANGE TEST AND
BLOCK COUNT
CODE IDENT
C
DWG NO
60297600
REV
AC
SHEET
LCM 3.4
PAGE
5-299

DETAILED-MODULES DIAGRAM
LCM CONTROL

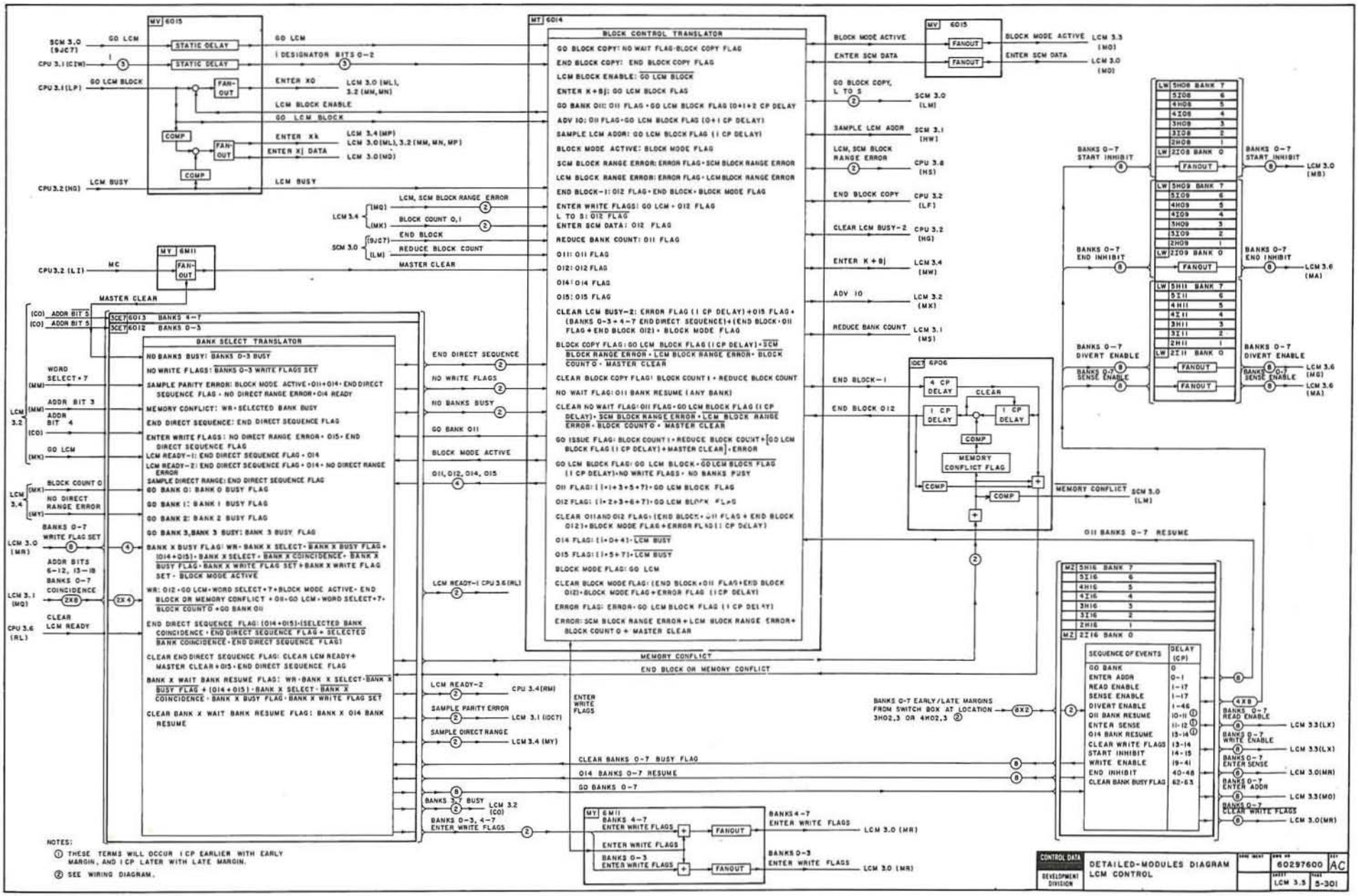
The control section of LCM determines the sequence of events during four CPU instructions. These are LCM to SCM Block Copy (011 instruction), SCM to LCM Block Copy (012 instruction), Read LCM to X (014 instruction), and Write X to LCM (015 instruction).

BANK SELECT AND SEQUENCE CONTROL

Control circuits in the 3CE7 modules select an LCM Bank and determine when a read/write cycle is to begin. Address Bits 3-5 are used to select the bank. A bank begins a read/write cycle when the Bank Select Translator (3CE7 modules) sends a Go Bank signal to one of the MZ modules. Each of these MZ modules controls the sequence of events for the corresponding LCM Bank.

BLOCK CONTROL

The Block Control Translator (MT module) generates signals which control LCM activity during block copy instructions. This module translates input signals received from the CPU, SCM, and LCM.


MV 6015
MT 6014
BLOCK CONTROL TRANSLATOR
BANK SELECT TRANSLATOR
MY 6011
IDCT 6P06
MZ 5H16 BANK 7
MZ 2I16 BANK 0
SEQUENCE OF EVENTS
DELAY (CP)
DETAILED-MODULES DIAGRAM
LCM CONTROL
CONTROL DATA
DEVELOPMENT DIVISION
60297600
AC
LCM 3.5
5-301

DETAILED-MODULES DIAGRAM
MEMORY STACKS AND ADDRESS DISTRIBUTION

Each LCM Bank contains a Bank Memory Stack in which 65,536 60-bit (plus parity) words are stored. This data is stored in magnetic cores which are arranged in a 512 x 512 x 16 array. Eight 60-bit words (plus parity bits) are read out or written into a stack simultaneously. Address Bits 6-18 determine which word group will be referenced during a given read/write cycle.

MEMORY STACKS

Each Bank Memory Stack contains 16 layers of vertically stacked planes. There are 512 word groups (eight 64-bit words) stored in each plane. A word group consists of a read/write drive line strung thru 512 cores. Read/write current entering the stack is applied to 16 of these drive lines on a single plane. However, a diode network diverts the current thru only one of the 16 drive lines.

A sense/inhibit line also passes thru the cores. There are 512 of these lines. Each line passes thru the same core (bit) of each word group in the stack. Therefore, a single sense/inhibit line passes thru 8,192 cores.

The Bank Memory Stacks are physically subdivided into planes, sectors, and quadrants. This simplifies trouble isolation procedures. (Refer to maintenance section.)

STACK ADDRESS

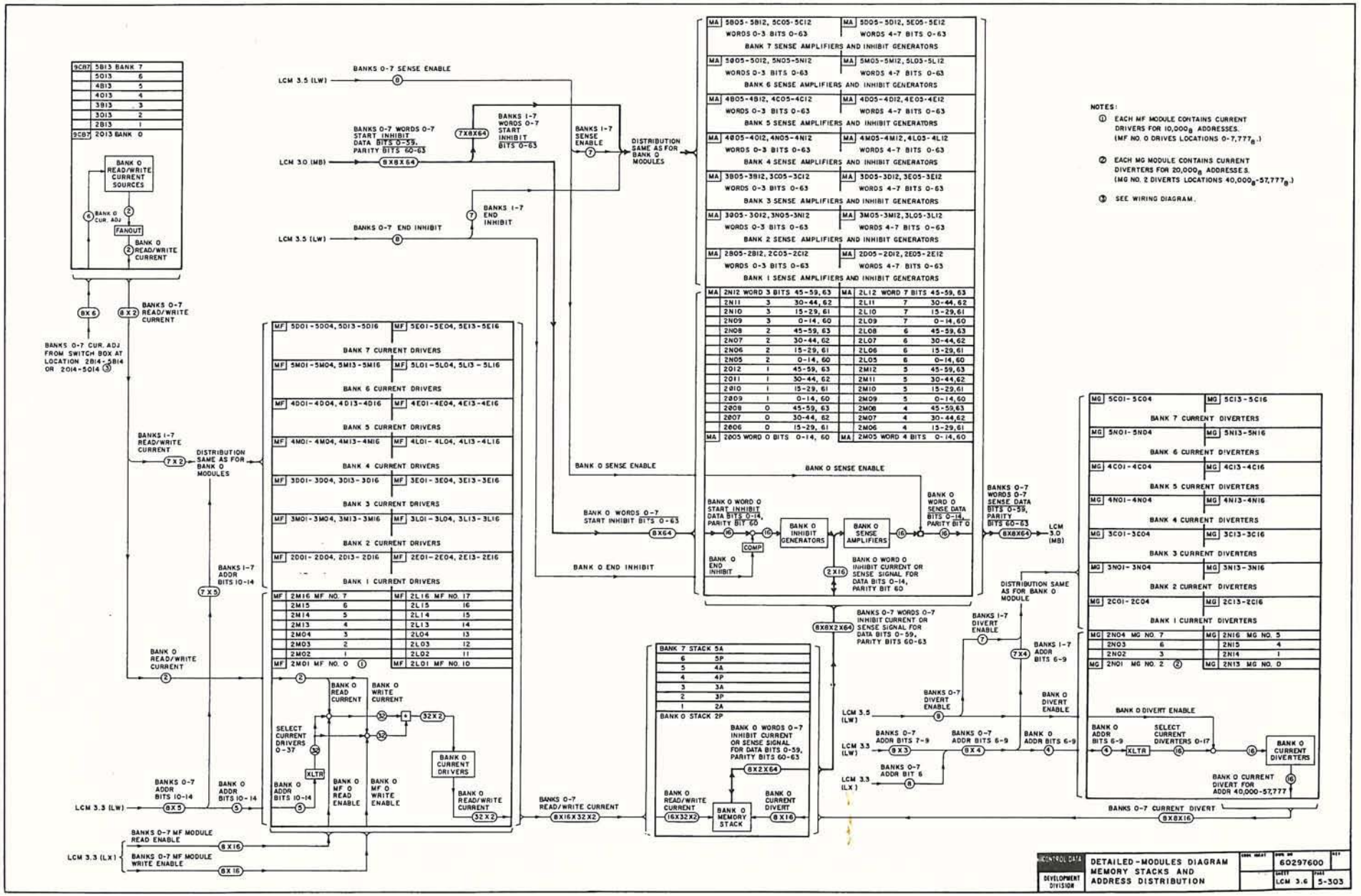
Address Bits 6-18 determine which word group is selected for a stack reference. Bits 15-18 select one of 16 MF modules to apply read/write current to a section of the stack. The selection is indicated by the MF Module Read Enable and MF Module Write Enable signals from an LX module. Bits 10-14 select one of 32 Bank Current Drivers (MF module) to apply read/write current to 16 drive lines in the stack. Bits 6-9 select one of 16 Bank Current Diverters in each of the MG modules. Each divert circuit is connected to two drive lines on all 16 planes. The divert circuit allows current to flow thru the correct read/write drive line.

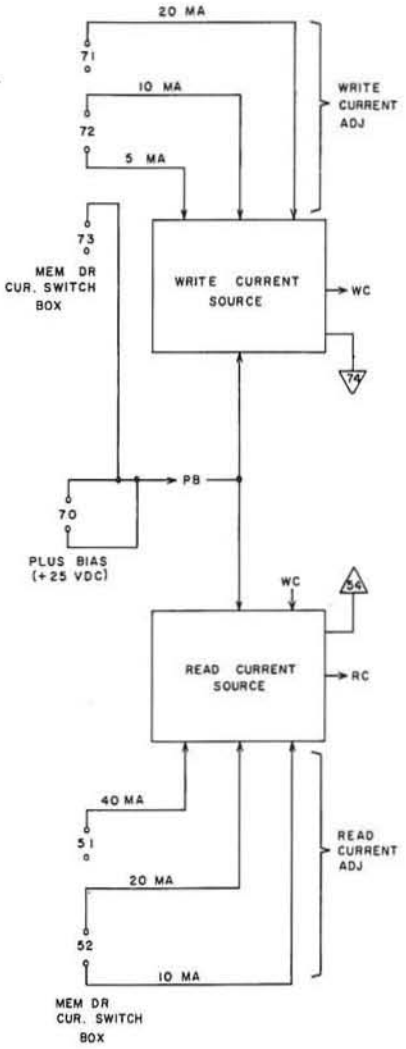
READ/SENSE

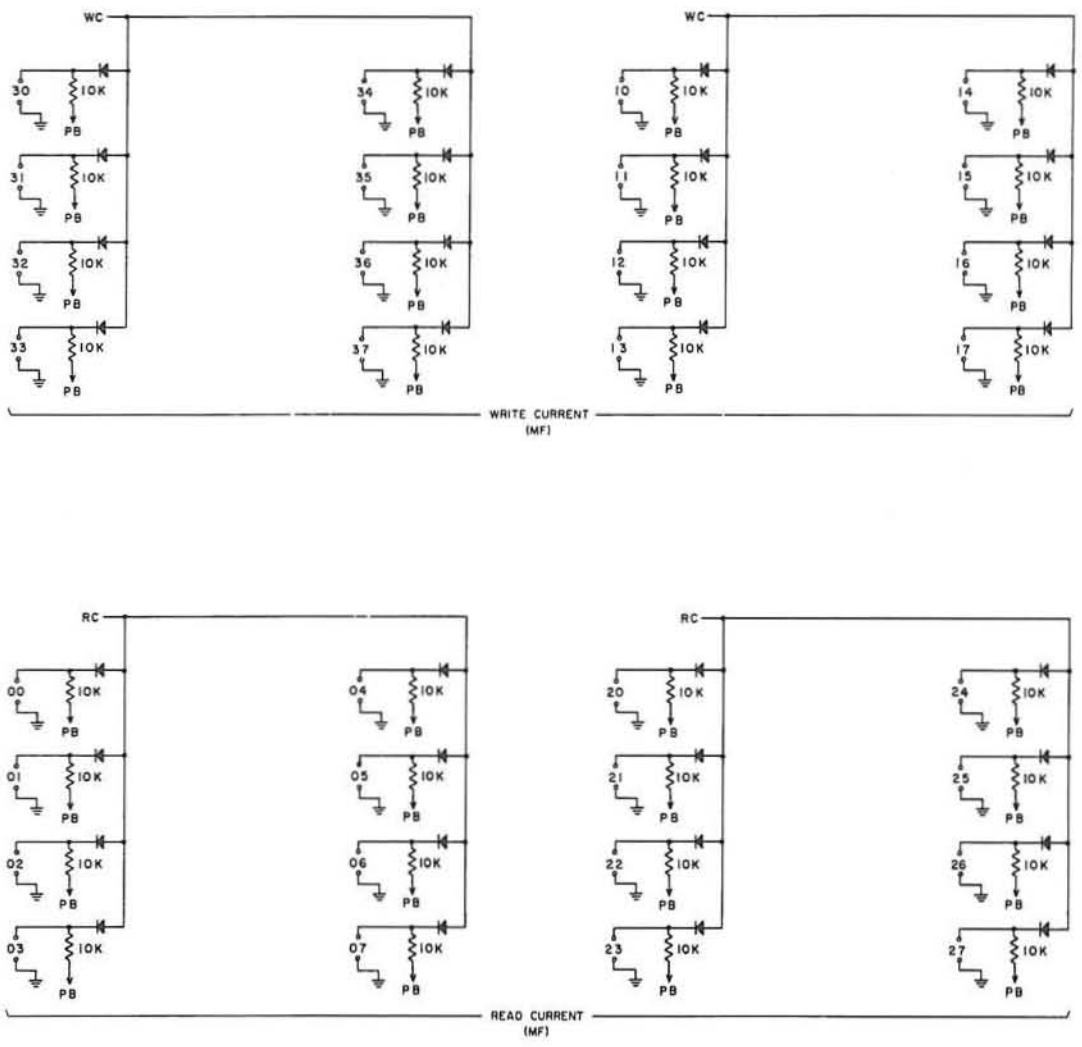
During the read portion of a bank read/write cycle, one Bank Current Driver (MF module) and eight Bank Current Diverters (MG modules) are enabled. (Only one diverter circuit is actually involved.) This allows read current to flow thru one drive line. All cores (bits) in the word group that are in a one state change to zeros. This change in state causes a signal to be transmitted thru the sense/inhibit lines to the Sense Amplifiers (MA modules). All cores that are in a zero state do not change. Therefore, no sense signal is generated. The Sense Amplifiers output complemented sense data to the Bank Operand Register (MB modules). This data is gated by a Bank Sense Enable signal from the Bank Sequence Control (via LW module). After a word group has been read from a stack, all cores in that location are in a zero state. However, the word group is restored during the write portion of the bank read/write cycle with the original data or new write data.

WRITE/INHIBIT

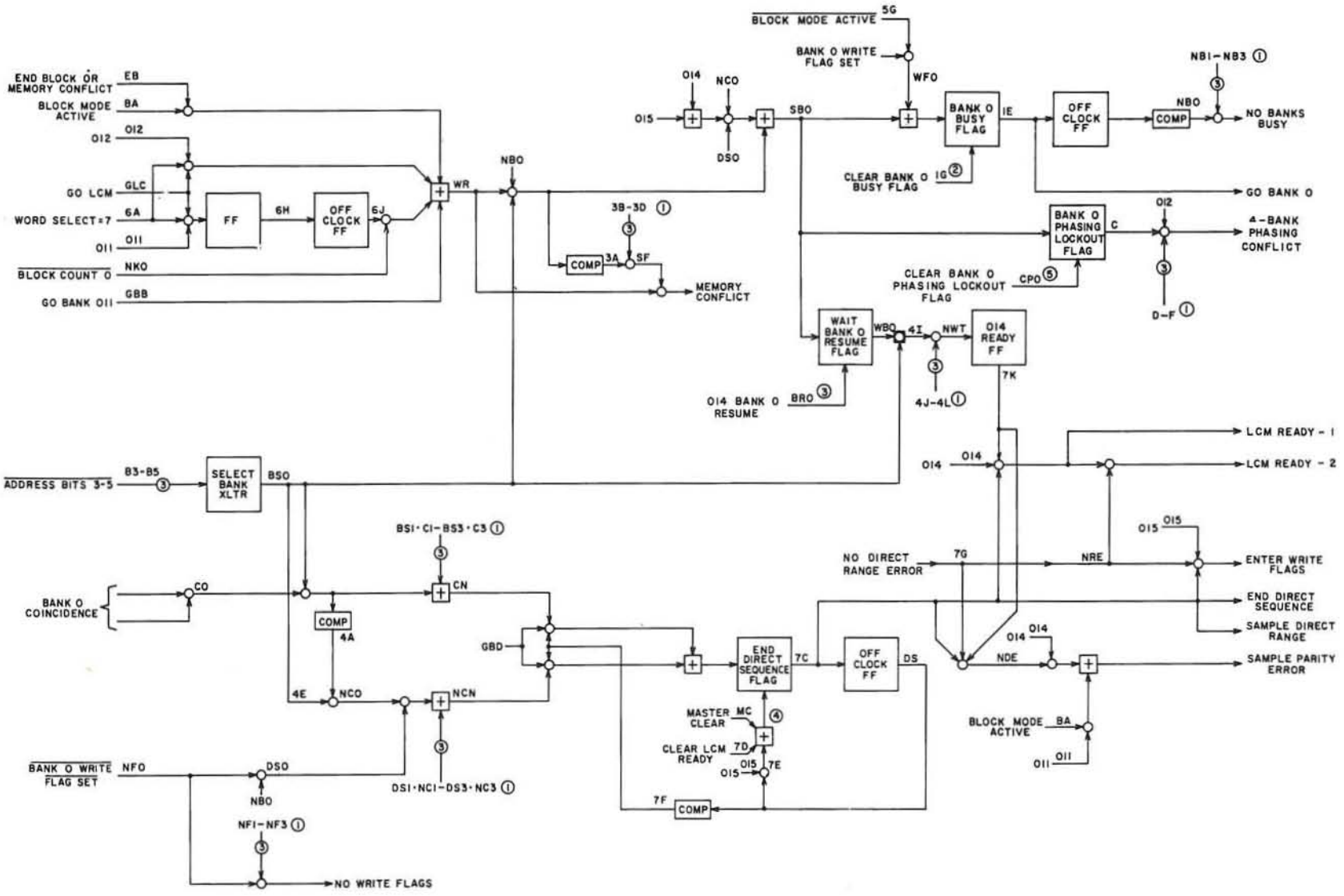
During the write portion of the cycle, current flows thru the read/write drive line in the opposite direction. Unless this current is unopposed, all cores in the word group change to a one state. Where a zero state is required, inhibit current is passed thru the appropriate sense/inhibit line. This current opposes the write current. The resultant current is not sufficient to switch the core to a one state. Inhibit data is held in the Bank Operand Register (MB modules). This data is the complement of write data and enables Bank Inhibit Generators (MA modules) to supply current to the sense/inhibit lines. The inhibit current flows until a Bank End Inhibit signal is generated by the Bank Sequence Control (via LW module).


NOTES:
① EACH MF MODULE CONTAINS CURRENT DRIVERS FOR 10,000₈ ADDRESSES. (MF NO. 0 DRIVES LOCATIONS 0-7,777₈.)
② EACH MG MODULE CONTAINS CURRENT DIVERTERS FOR 20,000₈ ADDRESSES. (MG NO. 2 DIVERTS LOCATIONS 40,000₈-57,777₈.)
③ SEE WIRING DIAGRAM.
BANK 7 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 6 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 5 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 4 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 3 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 2 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 1 SENSE AMPLIFIERS AND INHIBIT GENERATORS
BANK 7 CURRENT DRIVERS
BANK 6 CURRENT DRIVERS
BANK 5 CURRENT DRIVERS
BANK 4 CURRENT DRIVERS
BANK 3 CURRENT DRIVERS
BANK 2 CURRENT DRIVERS
BANK 1 CURRENT DRIVERS
BANK 7 CURRENT DIVERTERS
BANK 6 CURRENT DIVERTERS
BANK 5 CURRENT DIVERTERS
BANK 4 CURRENT DIVERTERS
BANK 3 CURRENT DIVERTERS
BANK 2 CURRENT DIVERTERS
BANK 1 CURRENT DIVERTERS
BANK 7 STACK 5A
BANK 0 STACK 2P
BANK 0 MEMORY STACK
BANK 0 READ/WRITE CURRENT SOURCES
BANK 0 CUR. ADJ
FANOUT
BANK 0 READ/WRITE CURRENT
BANKS 0-7 CUR. ADJ FROM SWITCH BOX AT LOCATION 2B14-5B14 OR 2D14-5D14 ③
BANKS 0-7 READ/WRITE CURRENT
BANKS 1-7 READ/WRITE CURRENT
BANKS 1-7 ADDR BITS 10-14
BANK 0 READ/WRITE CURRENT
BANKS 0-7 ADDR BITS 10-14
BANK 0 ADDR BITS 10-14
LCM 3.3 (LW)
LCM 3.3 (LX)
BANKS 0-7 MF MODULE READ ENABLE
BANKS 0-7 MF MODULE WRITE ENABLE
BANKS 0-7 SENSE ENABLE
LCM 3.5 (LW)
LCM 3.0 (MB)
BANKS 0-7 WORDS 0-7 START INHIBIT DATA BITS 0-59, PARITY BITS 60-63
BANKS 1-7 WORDS 0-7 START INHIBIT BITS 0-63
BANKS 1-7 SENSE ENABLE
DISTRIBUTION SAME AS FOR BANK 0 MODULES
BANKS 0-7 END INHIBIT
BANKS 1-7 END INHIBIT
BANK 0 SENSE ENABLE
BANK 0 WORDS 0-7 START INHIBIT BITS 0-63
BANK 0 END INHIBIT
BANK 0 WORD 0 START INHIBIT DATA BITS 0-14, PARITY BIT 60
BANK 0 INHIBIT GENERATORS
BANK 0 SENSE AMPLIFIERS
BANK 0 WORD 0 SENSE DATA BITS 0-14, PARITY BIT 0
COMP
BANK 0 END INHIBIT
BANK 0 WORD 0 INHIBIT CURRENT OR SENSE SIGNAL FOR DATA BITS 0-14, PARITY BIT 60
BANKS 0-7 WORDS 0-7 SENSE DATA BITS 0-59, PARITY BITS 60-63
BANKS 0-7 WORDS 0-7 INHIBIT CURRENT OR SENSE SIGNAL FOR DATA BITS 0-59, PARITY BITS 60-63
BANK 0 WORDS 0-7 INHIBIT CURRENT OR SENSE SIGNAL FOR DATA BITS 0-59, PARITY BITS 60-63
BANK 0 READ/WRITE CURRENT
BANK 0 CURRENT DIVERT
BANKS 0-7 READ/WRITE CURRENT
BANKS 0-7 CURRENT DIVERT
BANKS 1-7 DIVERT ENABLE
BANKS 0-7 DIVERT ENABLE
BANK 0 DIVERT ENABLE
BANKS 0-7 ADDR BITS 7-9
BANKS 0-7 ADDR BITS 6-9
BANK 0 ADDR BITS 6-9
BANKS 0-7 ADDR BIT 6
BANK 0 ADDR BITS 6-9
SELECT CURRENT DIVERTERS 0-17
BANK 0 CURRENT DIVERTERS
BANK 0 CURRENT DIVERT FOR ADDR 40,000-57,777
DISTRIBUTION SAME AS FOR BANK 0 MODULE
SELECT CURRENT DRIVERS 0-37
BANK 0 READ CURRENT
BANK 0 WRITE CURRENT
BANK 0 CURRENT DRIVERS
BANK 0 ADDR BITS 10-14
BANK 0 MF 0 READ ENABLE
BANK 0 MF 0 WRITE ENABLE
XLTR
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM MEMORY STACKS AND ADDRESS DISTRIBUTION
60297600
LCM 3.6
5-303





CONTROL DATA	9CB7 MODULE-LCM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	READ, WRITE CURRENT SOURCES	C	60297600	
		SHEET	PAGE 5-304.1	



NOTES:

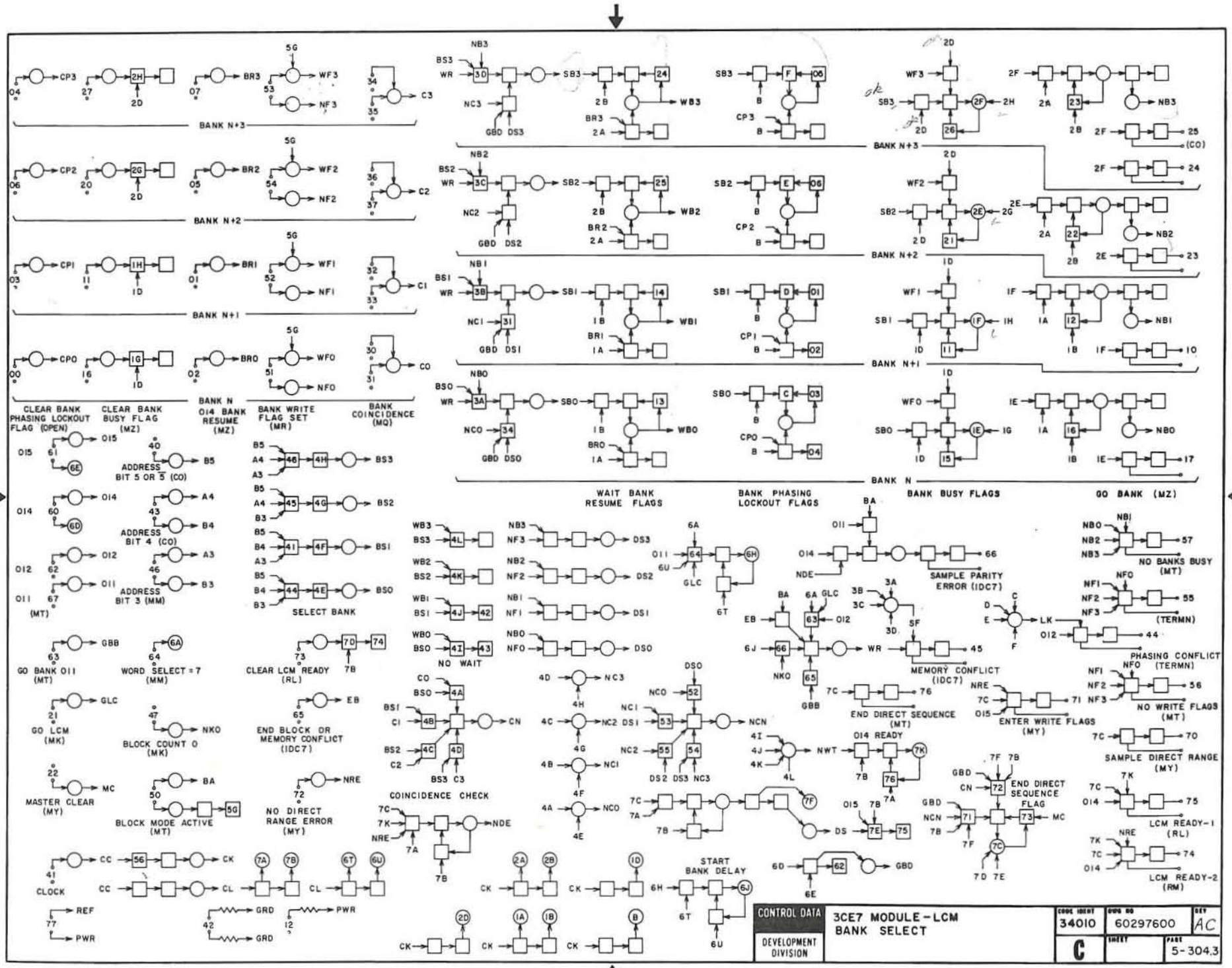
① FOR CLARITY, ONLY BANK 0 CIRCUITS ARE SHOWN.

② BANK 0 BUSY FLAG CLEARS WHEN 1G TERM IS A ZERO.

③ WAIT BANK 0 RESUME FLAG CLEARS WHEN BRO TERM IS A ONE AND CLOCK IS OFF.

④ END DIRECT SEQUENCE FLAG CLEARS WHEN ANY MC, 7D, OR 7E TERM IS A ZERO.

⑤ BANK 0 PHASING LOCKOUT FLAG CLEARS WHEN CPO TERM IS A ONE.


BANK N+3
BANK N+2
BANK N+1
BANK N
CLEAR BANK PHASING LOCKOUT FLAG (OPEN)
CLEAR BANK BUSY FLAG (MZ)
BANK N 014 BANK RESUME (MZ)
BANK WRITE FLAG SET (MR)
BANK COINCIDENCE (MQ)
WAIT BANK RESUME FLAGS
BANK PHASING LOCKOUT FLAGS
BANK BUSY FLAGS
GO BANK (MZ)
ADDRESS BIT 5 OR 5 (CO)
ADDRESS BIT 4 (CO)
ADDRESS BIT 3 (MM)
(MT)
SELECT BANK
GO BANK 011 (MT)
WORD SELECT = 7 (MM)
CLEAR LCM READY (RL)
GO LCM (MK)
BLOCK COUNT 0 (MK)
END BLOCK OR MEMORY CONFLICT (IDC7)
MASTER CLEAR (MY)
BLOCK MODE ACTIVE (MT)
NO DIRECT RANGE ERROR (MY)
NO WAIT
COINCIDENCE CHECK
BS3 C3
START BANK DELAY
SAMPLE PARITY ERROR (IDC7)
MEMORY CONFLICT (IDC7)
END DIRECT SEQUENCE (MT)
ENTER WRITE FLAGS (MY)
014 READY
END DIRECT SEQUENCE FLAG
NO BANKS BUSY (MT)
PHASING CONFLICT (TERMN)
NO WRITE FLAGS (MT)
SAMPLE DIRECT RANGE (MY)
LCM READY-1 (RL)
LCM READY-2 (RM)
CLOCK
REF
PWR
GRD
CONTROL DATA
DEVELOPMENT DIVISION
3CE7 MODULE - LCM
BANK SELECT
CODE IDENT 34010
DWG NO 60297600
REV AC
SIZE C
SHEET
PAGE 5-304.3

CO MODULE WIRING AT LOCATION 6011

FROM	ADDRESS	INPUT PIN	OUTPUT PIN	ADDRESS	TO
(MN)	BIT $\overline{18}$	54	44	BIT $\overline{18}$	(MX)
	$\overline{17}$	51	41	$\overline{17}$	
	$\overline{16}$	34	24	$\overline{16}$	
	$\overline{15}$	33	23	$\overline{15}$	
	$\overline{14}$	30	20	$\overline{14}$	
	$\overline{13}$	15	05	$\overline{13}$	
	$\overline{12}$	10	00	$\overline{12}$	
	18	53	43	18	(MQ)
	18	52	42	18	
	17	50	40	17	
	17	37	27	17	
	16	36	26	16	
	16	35	25	16	
	15	32	22	15	
	15	31	21	15	
	14	17	07	14	
	14	16	06	14	
	13	14	04	13	
	13	13	03	13	
	12	12	02	12	
	12	11	01	12	
(MM)	5	74	64	5	(MS)
"0"	–	65	–	–	–
"1" ①	–	75	–	–	–
–	–	–	63	–	TERMN
–	–	–	70	–	
–	–	–	60		
–	–	–	61		
–	–	–	62		
–	–	–	71		
–	–	–	72		
–	–	–	73		

INTER-MODULE WIRING

CO MODULE WIRING AT LOCATION 6010

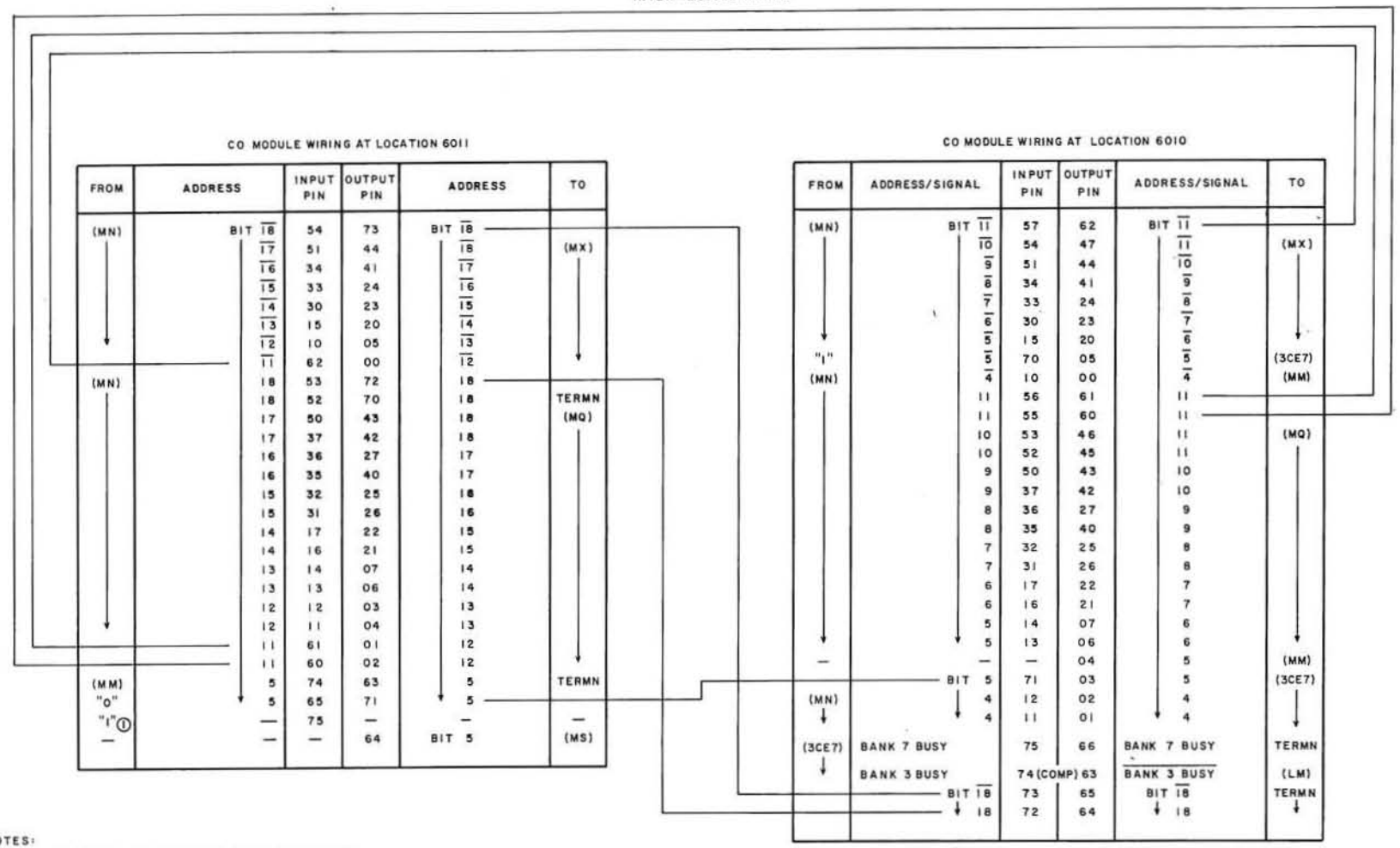
FROM	ADDRESS/SIGNAL	INPUT PIN	OUTPUT PIN	ADDRESS/SIGNAL	TO
(MN)	BIT $\overline{11}$	57	47	BIT $\overline{11}$	(MX)
	$\overline{10}$	54	44	$\overline{10}$	
	$\overline{9}$	51	41	$\overline{9}$	
	$\overline{8}$	34	24	$\overline{8}$	
	$\overline{7}$	33	23	$\overline{7}$	
	$\overline{6}$	30	20	$\overline{6}$	
	$\overline{5}$	15	05	$\overline{5}$	(3CE7)
	$\overline{4}$	10	00	$\overline{4}$	(MM)
	11	56	46	11	(MQ)
	11	55	45	11	
	10	53	43	10	
	10	52	42	10	
	9	50	40	9	
	9	37	27	9	
	8	36	26	8	
	8	35	25	8	
	7	32	22	7	
	7	31	21	7	
	6	17	07	6	
	6	16	06	6	
	5	14	04	5	(MM)
	5	13	03	5	(3CE7)
	4	12	02	4	
	4	11	01	4	
(3CE7)	BANK 7 BUSY	75	65	BANK 7 BUSY	TERMN
	BANK 3 BUSY	74	64	BANK 3 BUSY	
"1"	8-BANK PHASE ENABLE	70	63	8-BANK PHASE ENABLE	(LM)
–	–	–	66	–	TERMN
		60	–	–	–
		61	–	–	–
		62	–	–	–
		71	–	–	–
		72	–	–	–
		73	–	–	–

NOTES:

① LOGICAL "1" IS CONNECTED TO UPPER AND LOWER TERMINALS OF 6011-75.

CONTROL DATA DEVELOPMENT DIVISION	CO MODULES - LCM BANK PHASING NETWORK (BANKS 0-7)	CODE IDENT 34010	DWG NO 60297600	REV AC
		SIZE C	SHEET	PAGE 5-305

INTER-MODULE WIRING



CO MODULE WIRING AT LOCATION 6011

FROM	ADDRESS	INPUT PIN	OUTPUT PIN	ADDRESS	TO
(MN)	BIT $\overline{18}$	54	73	BIT $\overline{18}$	
	$\overline{17}$	51	44	$\overline{18}$	(MX)
	$\overline{16}$	34	41	$\overline{17}$	
	$\overline{15}$	33	24	$\overline{16}$	
	$\overline{14}$	30	23	$\overline{15}$	
	$\overline{13}$	15	20	$\overline{14}$	
	$\overline{12}$	10	05	$\overline{13}$	
	$\overline{11}$	62	00	$\overline{12}$	
(MN)	18	53	72	18	
	18	52	70	18	TERMN
	17	50	43	18	(MQ)
	17	37	42	18	
	16	36	27	17	
	16	35	40	17	
	15	32	25	18	
	15	31	26	16	
	14	17	22	15	
	14	16	21	15	
	13	14	07	14	
	13	13	06	14	
	12	12	03	13	
	12	11	04	13	
	11	61	01	12	
	11	60	02	12	
(MM)	5	74	63	5	TERMN
"0"	5	65	71	5	
"1"①	—	75	—	—	
—	—	—	64	BIT 5	(MS)

CO MODULE WIRING AT LOCATION 6010

FROM	ADDRESS/SIGNAL	INPUT PIN	OUTPUT PIN	ADDRESS/SIGNAL	TO
(MN)	BIT $\overline{11}$	57	62	BIT $\overline{11}$	
	$\overline{10}$	54	47	$\overline{11}$	(MX)
	$\overline{9}$	51	44	$\overline{10}$	
	$\overline{8}$	34	41	$\overline{9}$	
	$\overline{7}$	33	24	$\overline{8}$	
	$\overline{6}$	30	23	$\overline{7}$	
	$\overline{5}$	15	20	$\overline{6}$	
"1"	$\overline{5}$	70	05	$\overline{5}$	(3CE7)
(MN)	$\overline{4}$	10	00	$\overline{4}$	(MM)
	11	56	61	11	
	11	55	60	11	
	10	53	46	11	(MQ)
	10	52	45	11	
	9	50	43	10	
	9	37	42	10	
	8	36	27	9	
	8	35	40	9	
	7	32	25	8	
	7	31	26	8	
	6	17	22	7	
	6	16	21	7	
	5	14	07	6	
	5	13	06	6	
—	—	—	04	5	(MM)
	BIT 5	71	03	5	(3CE7)
(MN)	4	12	02	4	
	4	11	01	4	
(3CE7)	BANK 7 BUSY	75	66	BANK 7 BUSY	TERMN
	BANK 3 BUSY	74 (COMP)	63	BANK 3 BUSY	(LM)
	BIT $\overline{18}$	73	65	BIT $\overline{18}$	TERMN
	18	72	64	18	

NOTES:
① LOGICAL "1" IS CONNECTED TO UPPER AND LOWER TERMINALS OF 6011-75.

CONTROL DATA	CO MODULES – LCM	CODE IDENT 34010	DWG NO 60297600	REV AC
DEVELOPMENT DIVISION	BANK PHASING NETWORK (BANKS 0-3)	C	SHEET	PAGE 5-306.1

INTER-MODULE WIRING

CO MODULE WIRING AT LOCATION 6011

FROM	ADDRESS	INPUT PIN	OUTPUT PIN	ADDRESS	TO
(MN)	BIT $\overline{16}$	54	70	BIT $\overline{18}$	TERMN
	$\overline{17}$	51	44	$\overline{18}$	(MX)
	$\overline{16}$	34	41	$\overline{17}$	
	$\overline{15}$	33	24	$\overline{16}$	
	$\overline{14}$	30	23	$\overline{15}$	
	$\overline{13}$	15	20	$\overline{14}$	
	$\overline{12}$	10	05	$\overline{13}$	
	$\overline{11}$	62	00	$\overline{12}$	
(MN)	18	53	72	18	
	18	52	71	18	
	17	50	43	18	(MQ)
	17	37	42	18	
	16	36	27	17	
	16	35	40	17	
	15	32	25	16	
	15	31	26	16	
	14	17	22	15	
	14	16	21	15	
	13	14	07	14	
	13	13	06	14	
	12	12	03	13	
	12	11	04	13	
	11	61	01	12	
	11	60	02	12	
(MM)	5	74	63	5	TERMN
"1" ①	5	75	64	5	(MS)
"0"	$\overline{5}$	65	73	$\overline{5}$	

CO MODULE WIRING AT LOCATION 6010

FROM	ADDRESS/SIGNAL	INPUT PIN	OUTPUT PIN	ADDRESS/SIGNAL	TO
(MN)	BIT $\overline{11}$	57	62	BIT $\overline{11}$	
	$\overline{10}$	54	47	$\overline{11}$	(MX)
	$\overline{9}$	51	44	$\overline{10}$	
	$\overline{8}$	34	41	$\overline{9}$	
	$\overline{7}$	33	24	$\overline{8}$	
	$\overline{6}$	30	23	$\overline{7}$	
	$\overline{5}$	15	20	$\overline{6}$	
	$\overline{4}$	73	05	$\overline{5}$	(3CE7)
(MN)	11	10	00	$\overline{4}$	(MM)
	11	56	61	11	
	10	55	60	11	
	10	53	46	11	(MQ)
	9	52	45	11	
	9	50	43	10	
	8	37	42	10	
	8	36	27	9	
	7	35	40	9	
	7	32	25	8	
	6	31	26	8	
	6	17	22	7	
	5	16	21	7	
	5	14	07	6	
"1"	5	13	06	6	
—	—	70	04	5	(MM)
(MN)	4	—	03	5	(3CE7)
	4	12	02	4	
(3CE7)	BANK 7 BUSY	11	01	4	
	BANK 3 BUSY	75 (COMP)	63	$\overline{\text{BANK 7 BUSY}}$	(LM)
	BIT 18	74	66	BANK 3 BUSY	TERMN
		72	64	BIT 18	
		71	65		

NOTES:

① LOGICAL "1" IS CONNECTED TO UPPER AND LOWER TERMINALS OF 6011-75.

CONTROL DATA DEVELOPMENT DIVISION	CO MODULES – LCM BANK PHASING NETWORK (BANKS 4–7)	EDOC IDENT 34010	DWG NO 60297600	REV AC
		SIZE C	SHEET	PAGE 5-306.3

This page has been left blank intentionally. The CS module has been replaced by the 9CB7 module.

READ DATA SELECT AND FAN-IN

The 1DC7 module selects Odd or Even Word Read Parity Bit 63 from one of eight Bank Operand Registers (MB modules). Bits 0, 3, 4, and 5 of the address determine which Read Parity Bit 63 will be output.

When a word has been selected, only one of the AND-NOT gates will have a meaningful output (one or zero). The remaining gates will output ones. Consequently, three of the four AND gates will be made and the remaining gate will determine the condition (one or zero) of the output bit. If all four AND gates are made (LO, MO, NO, and OO terms are all ones), the final AND-NOT gate will be made and the output bit will be a zero. If one of these terms is a zero, the gate will be broken and the output bit will be a one.

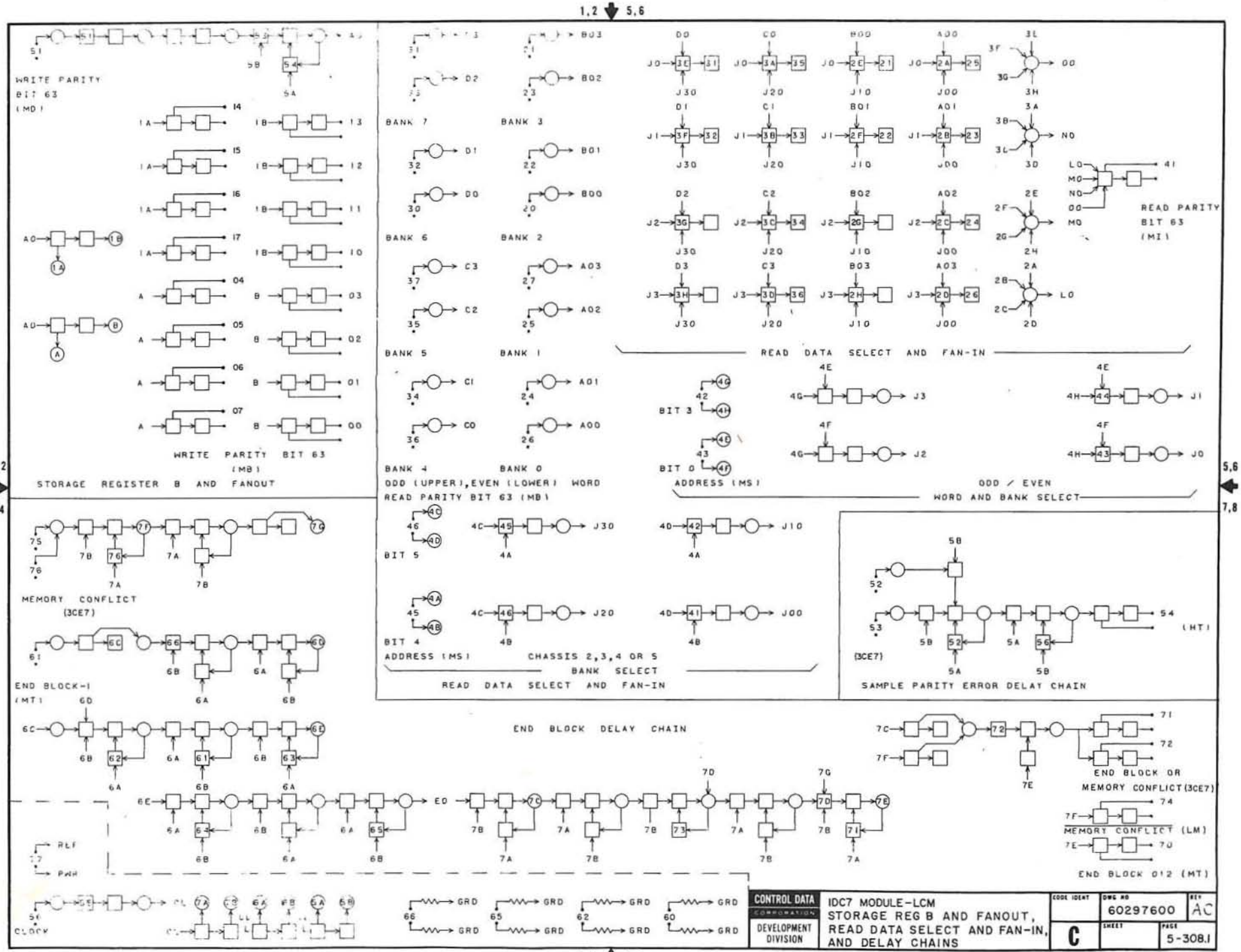
END BLOCK DELAY CHAIN

MEMORY CONFLICT

Two Memory Conflict signals are applied to an AND gate. This gate actually performs an OR function. One of the inputs will always be a one. The other input will be a one only if the selected bank is busy. If the AND gate is made, the End Block 012 signal will be disabled because the 7G term will be a zero.

END BLOCK

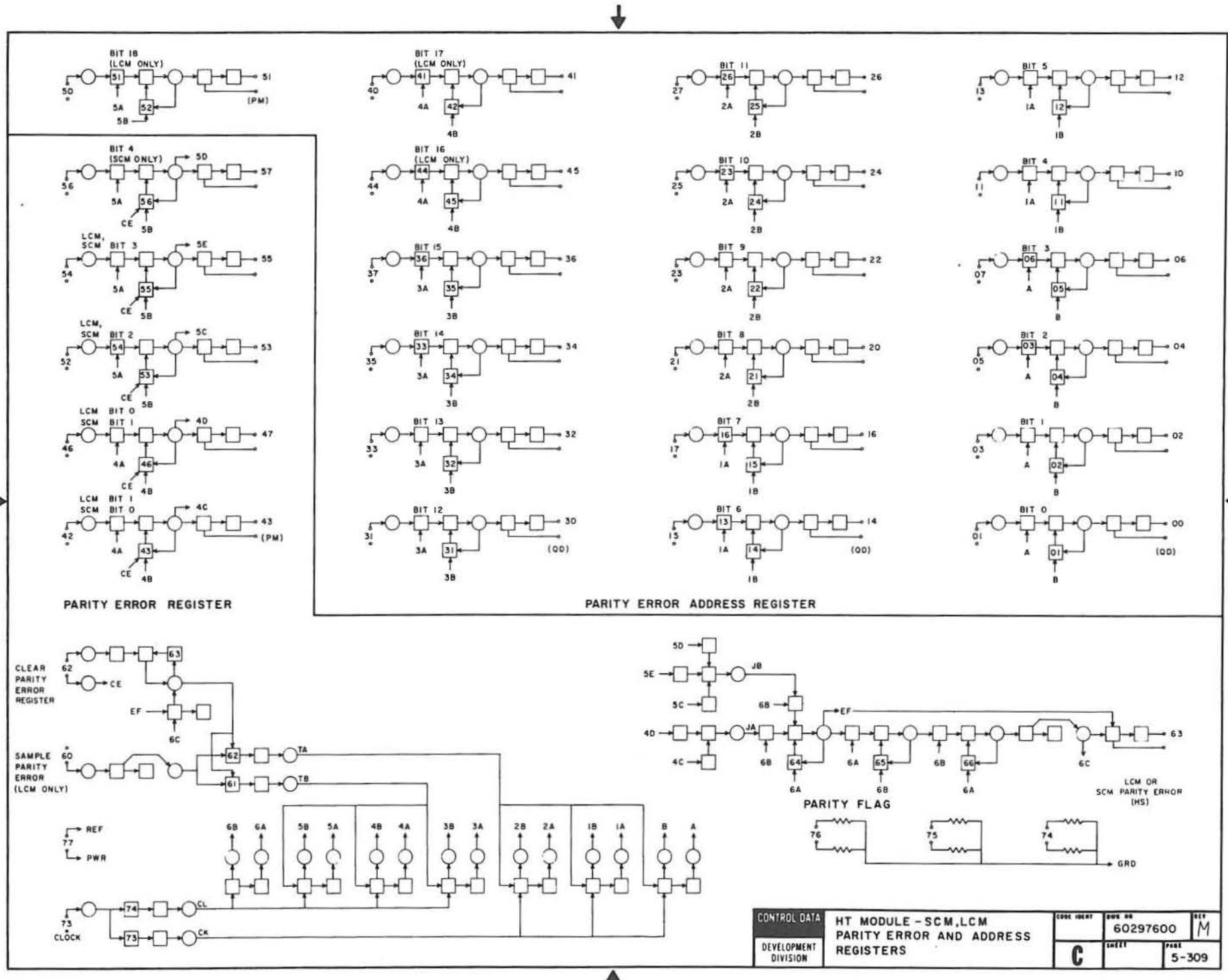
The End Block-1 input signal is delayed for six clock periods. If no memory conflicts occur, the End Block 012 output signal will be generated six clock periods after the End Block-1 input signal has arrived.

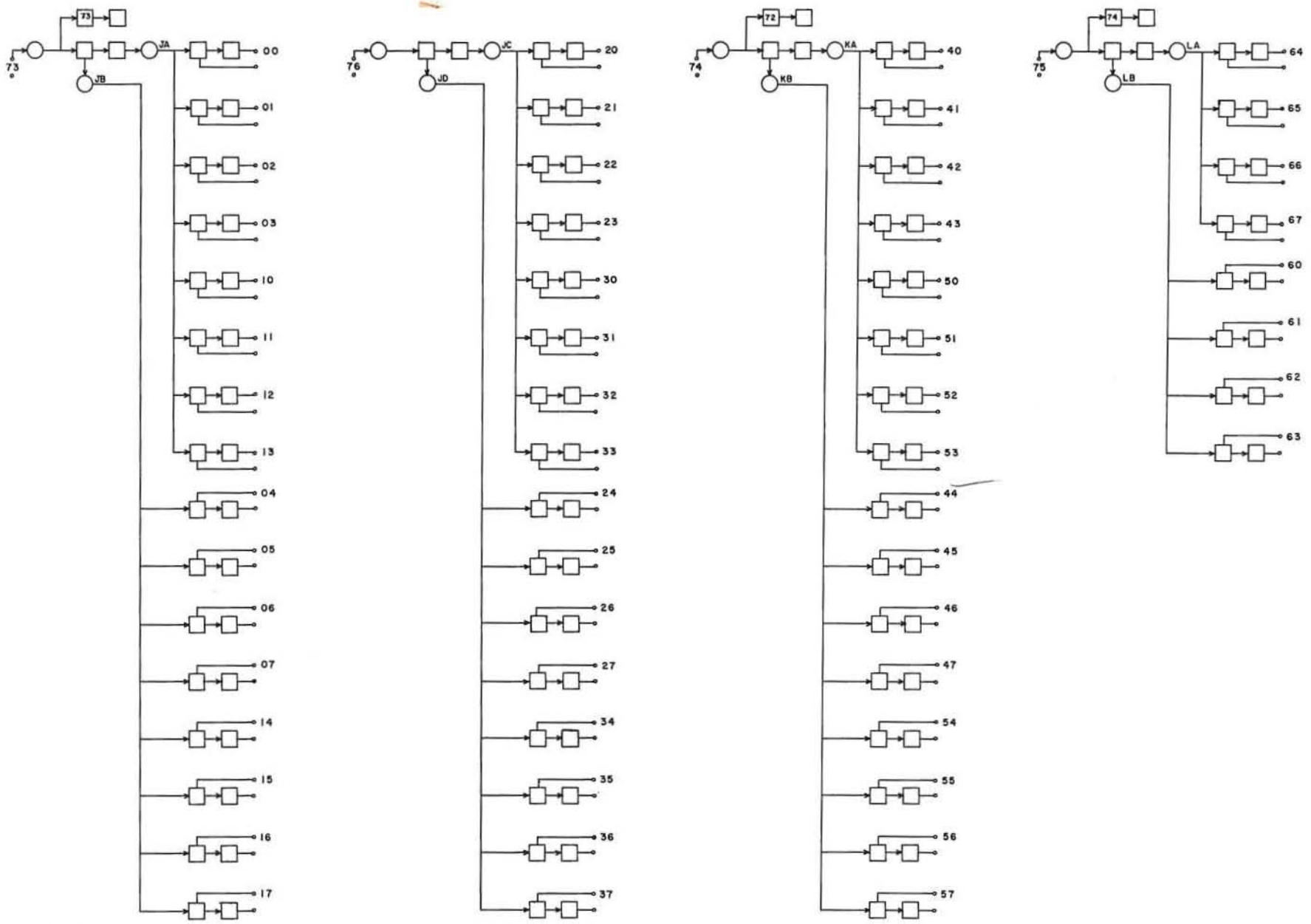

1,2
5,6
3,4
7,8
WRITE PARITY BIT 63 (MD)
STORAGE REGISTER B AND FANOUT
WRITE PARITY BIT 63 (MB)
BANK 7
BANK 3
BANK 6
BANK 2
BANK 5
BANK 1
BANK 4
BANK 0
ODD (UPPER), EVEN (LOWER) WORD READ PARITY BIT 63 (MB)
READ DATA SELECT AND FAN-IN
READ PARITY BIT 63 (MI)
BIT 3 ADDRESS (MS)
BIT 0 ADDRESS (MS)
ODD / EVEN WORD AND BANK SELECT
BIT 5
BIT 4 ADDRESS (MS)
CHASSIS 2,3,4 OR 5 BANK SELECT
READ DATA SELECT AND FAN-IN
SAMPLE PARITY ERROR DELAY CHAIN
(MT)
(3CE7)
MEMORY CONFLICT (3CE7)
END BLOCK-1 (MT)
END BLOCK DELAY CHAIN
END BLOCK OR MEMORY CONFLICT (3CE7)
MEMORY CONFLICT (LM)
END BLOCK 012 (MT)
RLF
PWR
CLOCK
GRD
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
IDC7 MODULE-LCM
STORAGE REG B AND FANOUT, READ DATA SELECT AND FAN-IN, AND DELAY CHAINS
CODE IDENT C
DWG NO 60297600
REV AC
SHEET
PAGE 5-308.1

HT MODULE

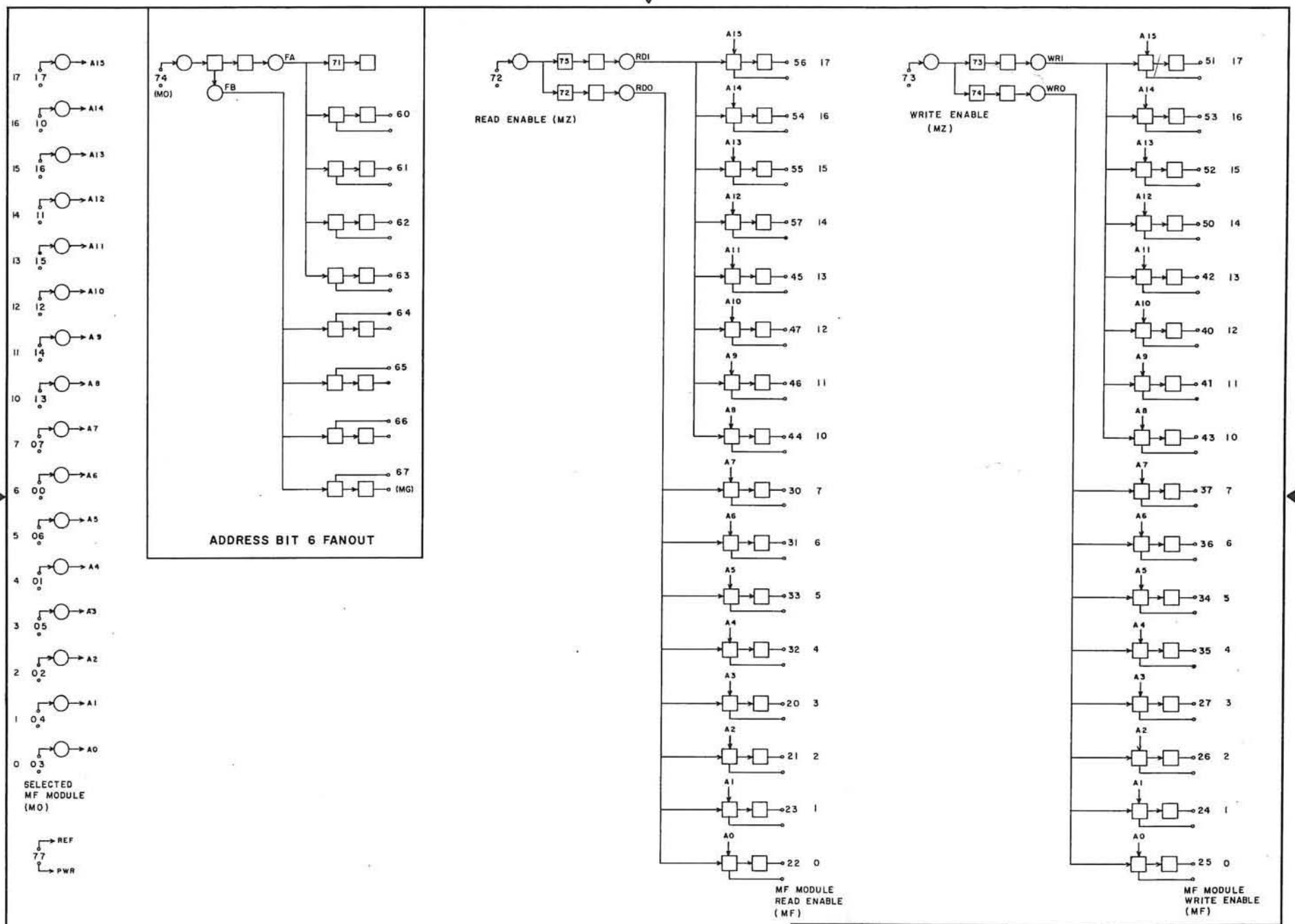
The HT module contains a four-bit LCM Parity Error Register and a 19-bit LCM Parity Error Address Register. Both registers are normally cleared and entered with new information every clock period under gated clock pulse control. This occurs when no parity errors exist in the word read from LCM. When no errors exist, the Parity Flag will be clear and the bit holding register (test point 63) will be set. The AND gates will be made (TA and TB terms present) to enable the clocks when the Sample Parity Error signal is present.

If any of the LCM Parity Error Register bits are set during a given clock period, the Parity Flag will set. This clears the bit holding register (test point 63) since both EF and 6C terms will be present for one clock period. Therefore, the AND gates will be broken (TA and TB terms absent) and the clock pulses will be disabled. At this time, the LCM Parity Error Address Register will contain the address in LCM at which an error has occurred. Also, the Parity Error Register will indicate which section of the 60-bit word has been misread from memory. Normal operation will be restored when the Clear Parity Error Register signal is applied.


BIT 18 (LCM ONLY)
BIT 17 (LCM ONLY)
BIT 16 (LCM ONLY)
BIT 15
BIT 14
BIT 13
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
BIT 4 (SCM ONLY)
LCM, SCM BIT 3
LCM, SCM BIT 2
LCM SCM BIT 0
LCM SCM BIT 1
LCM BIT 1 SCM BIT 0
(PM)
(QD)
CE
PARITY ERROR REGISTER
PARITY ERROR ADDRESS REGISTER
CLEAR PARITY ERROR REGISTER
SAMPLE PARITY ERROR (LCM ONLY)
REF
PWR
CLOCK
CL
CK
TA
TB
EF
JA
JB
PARITY FLAG
LCM OR SCM PARITY ERROR (HS)
GRD
CONTROL DATA
DEVELOPMENT DIVISION
HT MODULE - SCM, LCM PARITY ERROR AND ADDRESS REGISTERS
CODE IDENT
C
DWG NO
60297600
REV
M
SHEET
PAGE
5-309



CONTROL DATA	LW MODULE-LCM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	FANOUTS	C	60297600	
		SHEET	PAGE	5-311



MF MODULE READ/WRITE SELECT

CONTROL DATA DEVELOPMENT DIVISION	LX MODULE-LCM MF MODULE READ/WRITE SELECT AND ADDRESS BIT 6 FANOUT	CODE IDENT C	DWG NO 60297600	REV
			SHEET	PAGE 5-313

SENSE AMPLIFIERS AND INHIBIT GENERATORS

The MA module contains Sense Amplifiers and Inhibit Generators for 15 data bits and one parity bit. One of each is connected to a single sense/inhibit line in an LCM stack.

SENSE AMPLIFIERS

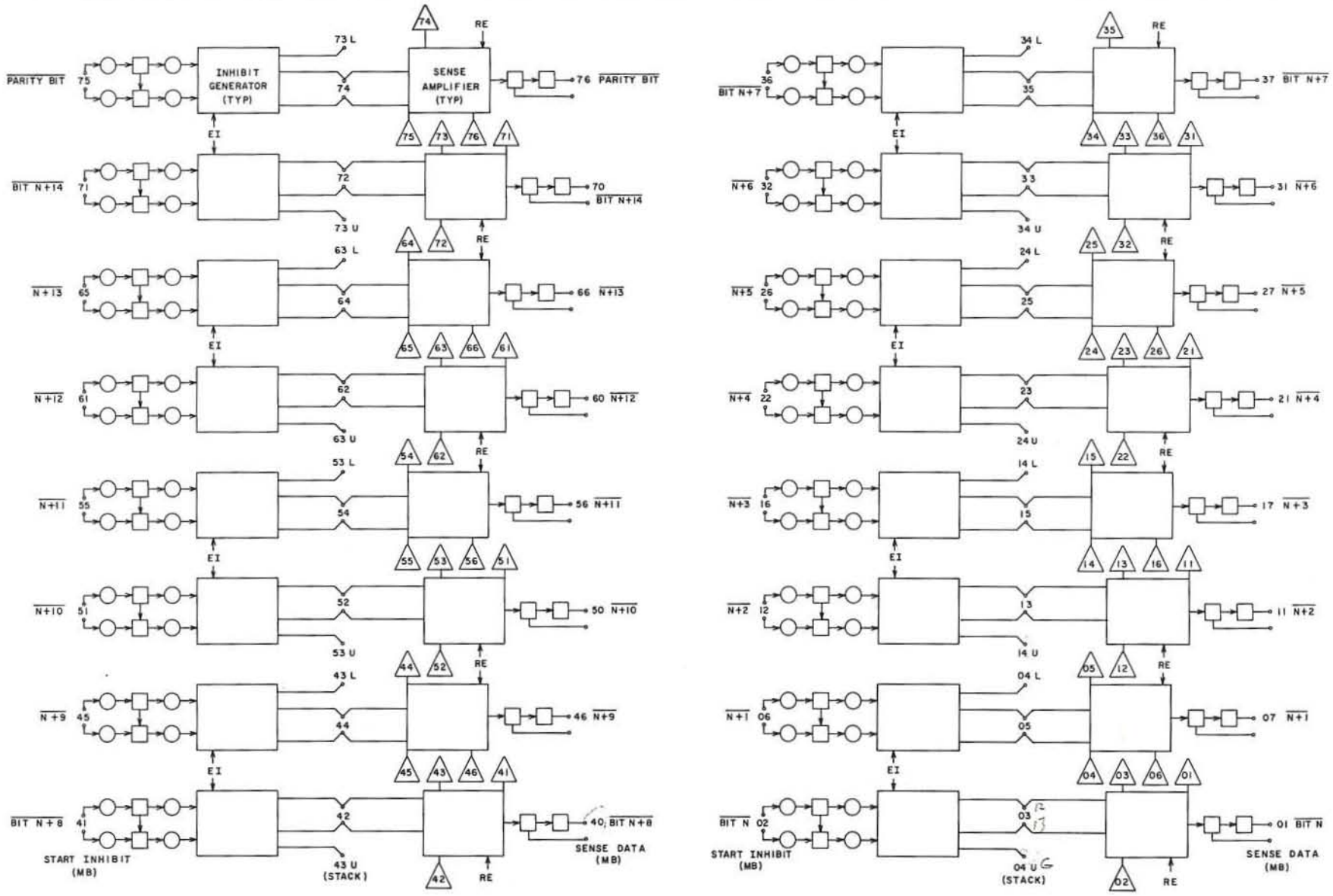
Each Sense Amplifier receives an input signal when a one has been read from the addressed core (bit) in the stack. These signals are filtered, amplified, and gated to the Bank Operand Register (MB modules) when Sense Enable is present. Test points are arranged as follows:

Test Point	Description
X3 or X4	Input signal before filter
X2 or X5	Input signal after filter
X1 or X6	Input signal after filter (opposite polarity from X2 or X5)

INHIBIT GENERATORS

Each Inhibit Generator passes current thru a sense/inhibit line when a zero is to be written into the addressed core (bit). Current begins to flow when the input bit from the Bank Operand Register (MB modules) is a one (complemented zero). Current stops flowing when End Inhibit is present.

Inhibit current does not flow directly thru a sense/inhibit line. Two identical currents flow simultaneously. One current passes thru the cores in planes 1-8. A second current passes thru the cores in planes 9-16. The third output wire shown in the diagram carries the total inhibit current.



CONTROL DATA	MA MODULE - LCM SENSE AMPLIFIERS AND INHIBIT GENERATORS	CODE IDENT	DWG NO 60297600 REV 11
DEVELOPMENT DIVISION		C	SHEET PAGE 5-315

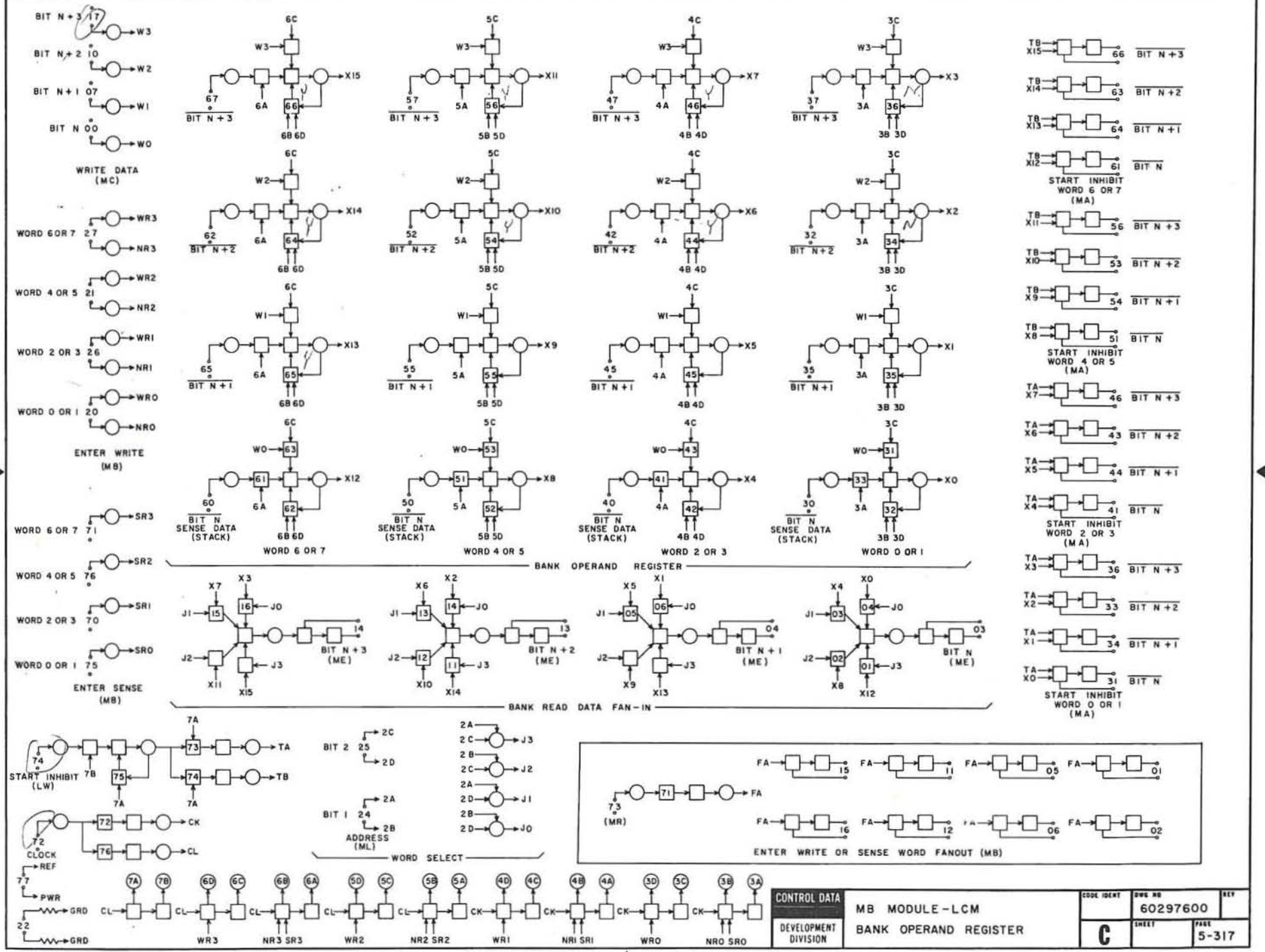
BANK OPERAND REGISTER

The Bank Operand Register is divided into eight 64-bit word sections (60 data bits plus four parity bits). It is contained within 32 MB modules. Half of these modules contain the word sections for odd-numbered words. The other half contains even-numbered word sections. Therefore, each MB module contains four bits of an even or odd word section of the register. The register holds the complement of either sense data from an LCM stack or write data from Storage Register B (MC modules).

Prior to initiation of the bank read/write cycle, write data enters the word sections when the corresponding Word Enter Write signals appear. Only one write data word can enter the register in a given clock period. When data is entered by a Word Enter Write signal, the corresponding Word Enter Sense signal will not appear during the following bank read cycle.

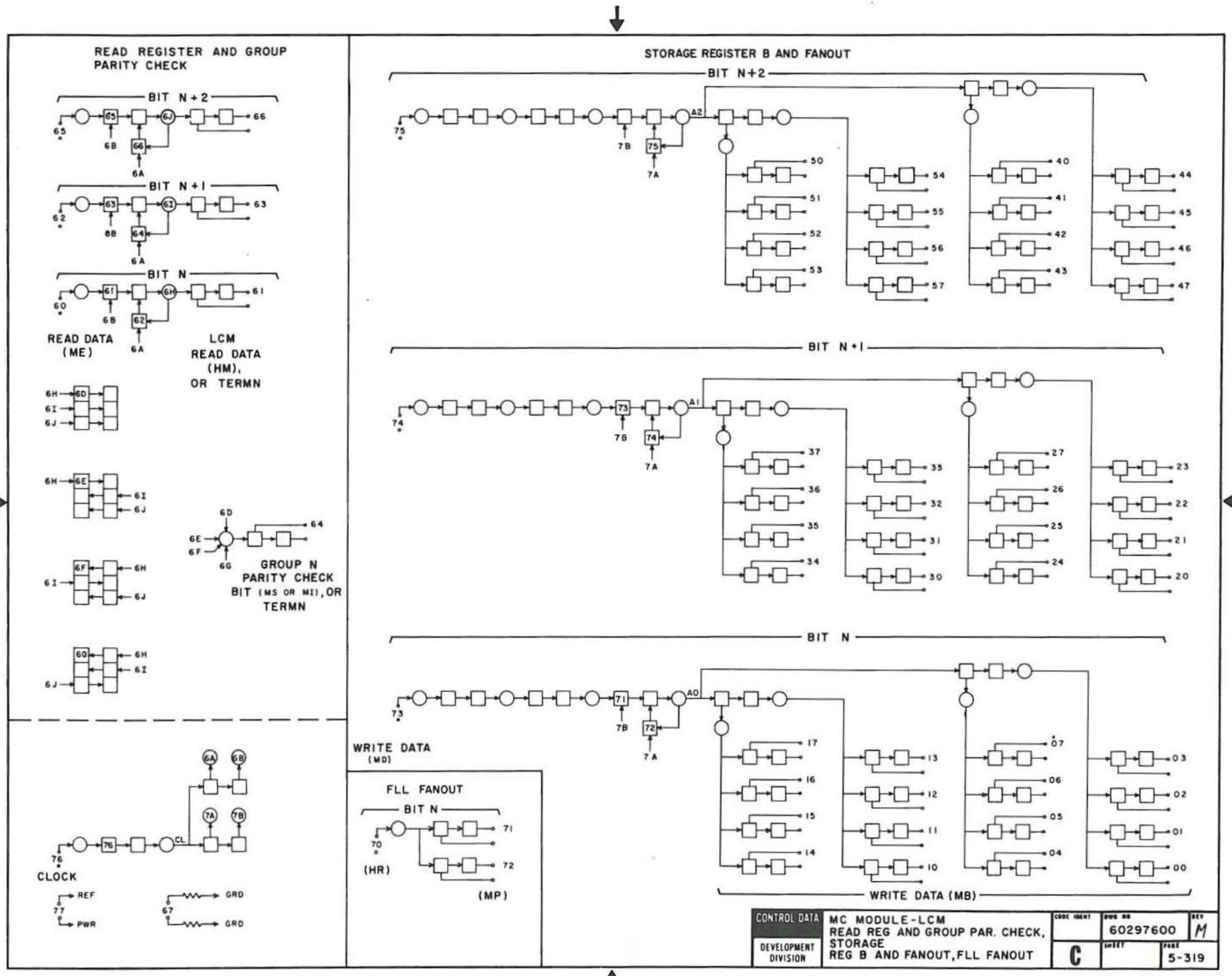
During the bank read cycle, sense data enters the word sections in which the corresponding Word Enter Sense signals are present and Word Enter Write signals are absent. Sense data enters all selected word sections during the same clock period. This data is recomplemented before being sent to the Read Data Select and Fan-in network (ME and 1DC7 modules). Only one read data word is output every clock period from each odd and even word section. The selected word is determined by the condition of bits 1 and 2 of the address.

When the Bank Sequence Control (MZ module) has generated a Bank Start Inhibit signal, all data in the Bank Operand Register is sent simultaneously to the Bank Inhibit Generators (MA modules). This causes new data to be written and/or sense data to be restored in an LCM stack. Data remains held in the register until a subsequent bank reference causes the word sections to clear and be entered with new sense or write data.


BIT N+3 17
BIT N+2 10
BIT N+1 07
BIT N 00
WRITE DATA (MC)
WORD 6 OR 7 27
WORD 4 OR 5 21
WORD 2 OR 3 26
WORD 0 OR 1 20
ENTER WRITE (MB)
WORD 6 OR 7 71
WORD 4 OR 5 76
WORD 2 OR 3 70
WORD 0 OR 1 75
ENTER SENSE (MB)
BIT N SENSE DATA (STACK)
WORD 6 OR 7
WORD 4 OR 5
WORD 2 OR 3
WORD 0 OR 1
BANK OPERAND REGISTER
BANK READ DATA FAN-IN
START INHIBIT WORD 6 OR 7 (MA)
START INHIBIT WORD 4 OR 5 (MA)
START INHIBIT WORD 2 OR 3 (MA)
START INHIBIT WORD 0 OR 1 (MA)
START INHIBIT (LW)
CLOCK REF
PWR
GRD
BIT 2 25
BIT 1 24
ADDRESS (ML)
WORD SELECT
ENTER WRITE OR SENSE WORD FANOUT (MB)
WR3 NR3 SR3 WR2 NR2 SR2 WR1 NR1 SR1 WRO NRO SRO
CONTROL DATA
DEVELOPMENT DIVISION
MB MODULE - LCM
BANK OPERAND REGISTER
CODE IDENT C
DWG NO 60297600
SHEET
PAGE 5-317

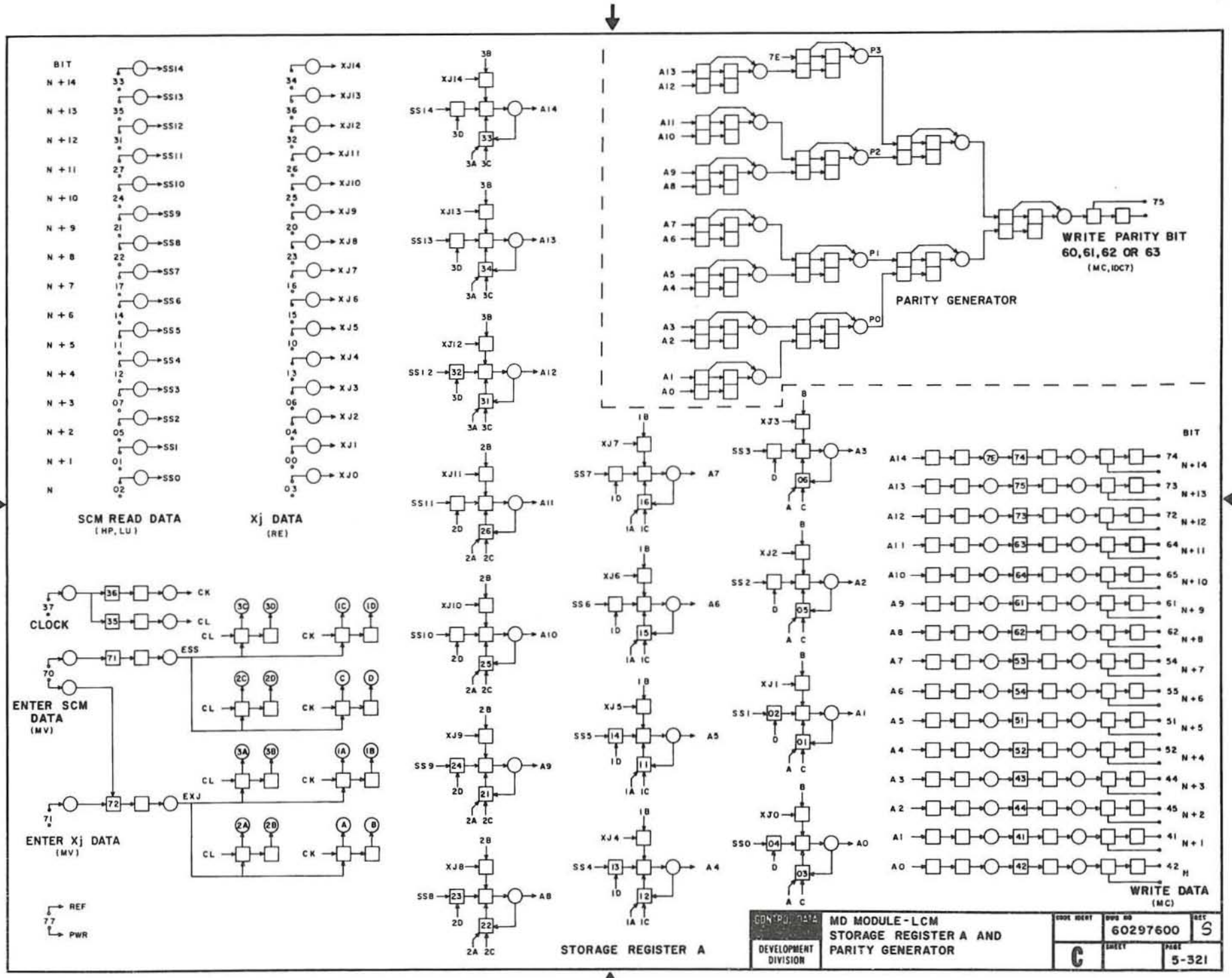
GROUP PARITY CHECK

The MC module checks the condition of the three-bit group which is stored in the Read Register. If an odd number of ones exist, the Group Parity Check Bit will be a one. When this occurs, one of the terms 6D, 6E, 6F, or 6G will be a zero. This breaks the AND gate. Consequently, the complemented output will be a one.


READ REGISTER AND GROUP PARITY CHECK
BIT N+2
BIT N+1
BIT N
READ DATA (ME)
LCM READ DATA (HM), OR TERMN
GROUP N PARITY CHECK BIT (MS OR MI), OR TERMN
CLOCK
REF
PWR
GRD
GRD
STORAGE REGISTER B AND FANOUT
BIT N+2
BIT N+1
BIT N
WRITE DATA (MD)
FLL FANOUT
BIT N
(HR)
(MP)
WRITE DATA (MB)
CONTROL DATA
DEVELOPMENT DIVISION
MC MODULE-LCM
READ REG AND GROUP PAR. CHECK, STORAGE
REG B AND FANOUT, FLL FANOUT
C
60297600
M
5-319

PARITY GENERATOR

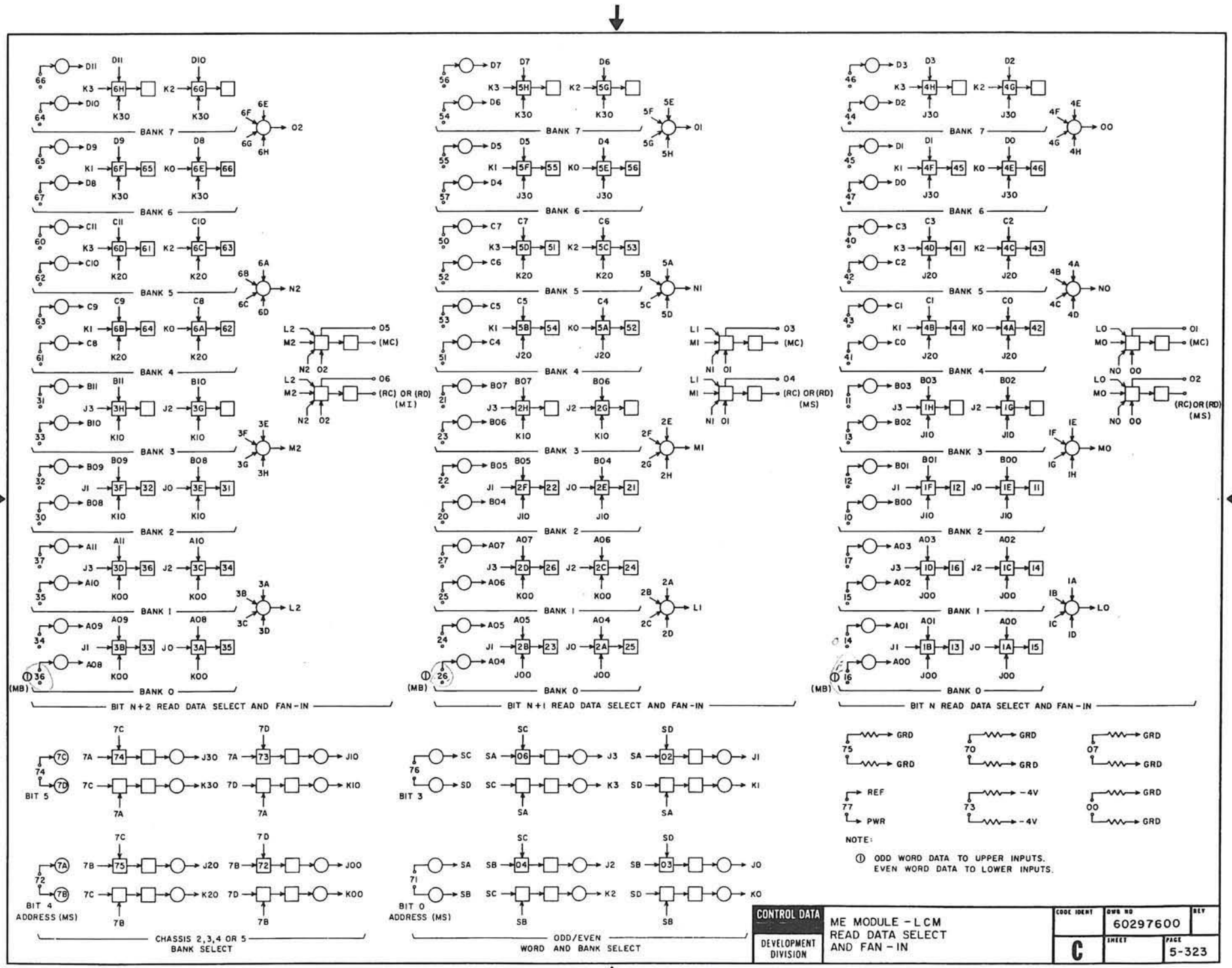
The MD module checks the condition of the 15-bit word section which is stored in Storage Register A. If an even number of ones exist, the Write Parity Bit will be a one. If an odd number of ones exist, this bit will be a zero. The check is made in a series of EXCLUSIVE OR gates. The lower group of gates checks the parity of the lower eight bits. The upper group checks the upper seven bits. If odd parity exists in one group and even parity exists in the other group, the final gate will be made and the complemented output will be a zero. If both groups contain odd or even parity, the final gate will be broken and the complemented output will be a one.


SCM READ DATA
(HP, LU)
Xj DATA
(RE)
CLOCK
ENTER SCM DATA
(MV)
ENTER Xj DATA
(MV)
REF
PWR
STORAGE REGISTER A
PARITY GENERATOR
WRITE PARITY BIT
60,61,62 OR 63
(MC, IDC7)
WRITE DATA
(MC)
MD MODULE - LCM
STORAGE REGISTER A AND
PARITY GENERATOR
CONTROL DATA
DEVELOPMENT DIVISION
60297600
C
5-321

READ DATA SELECT AND FAN-IN

The ME modules utilize bits 0, 3, 4, and 5 of the address to select an odd or even word from one of eight Bank Operand Registers (MB modules). Each module contains the selection network for three bits of the word. The following description pertains to the network for the lowest order bit.

When a word has been selected, only one of the AND-NOT gates will have a meaningful output (one or zero). The remaining gates will output ones. Consequently, three of the four AND gates will be made and the remaining gate will determine the condition (one or zero) of the output bit. If all four AND gates are made (LO, MO, NO, and OO terms are all ones), the final AND-NOT gate will be made and the output bit will be a zero. If one of these terms is a zero, the gate will be broken and the output bit will be a one.



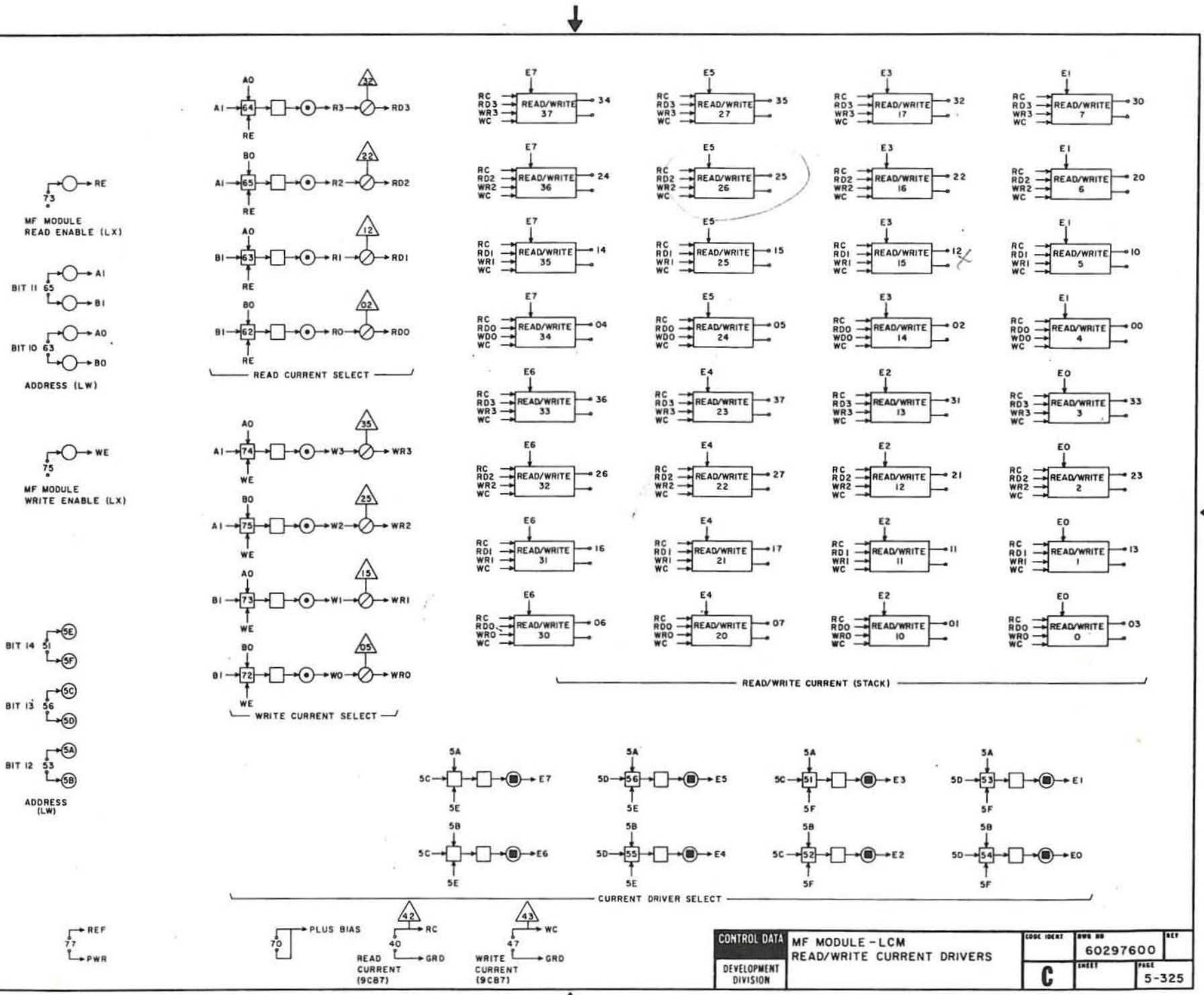
CONTROL DATA
DEVELOPMENT DIVISION

ME MODULE - LCM
READ DATA SELECT
AND FAN - IN

CODE IDENT: C
DWG NO: 60297600
REV:
SHEET:
PAGE: 5-323

READ/WRITE CURRENT DRIVERS

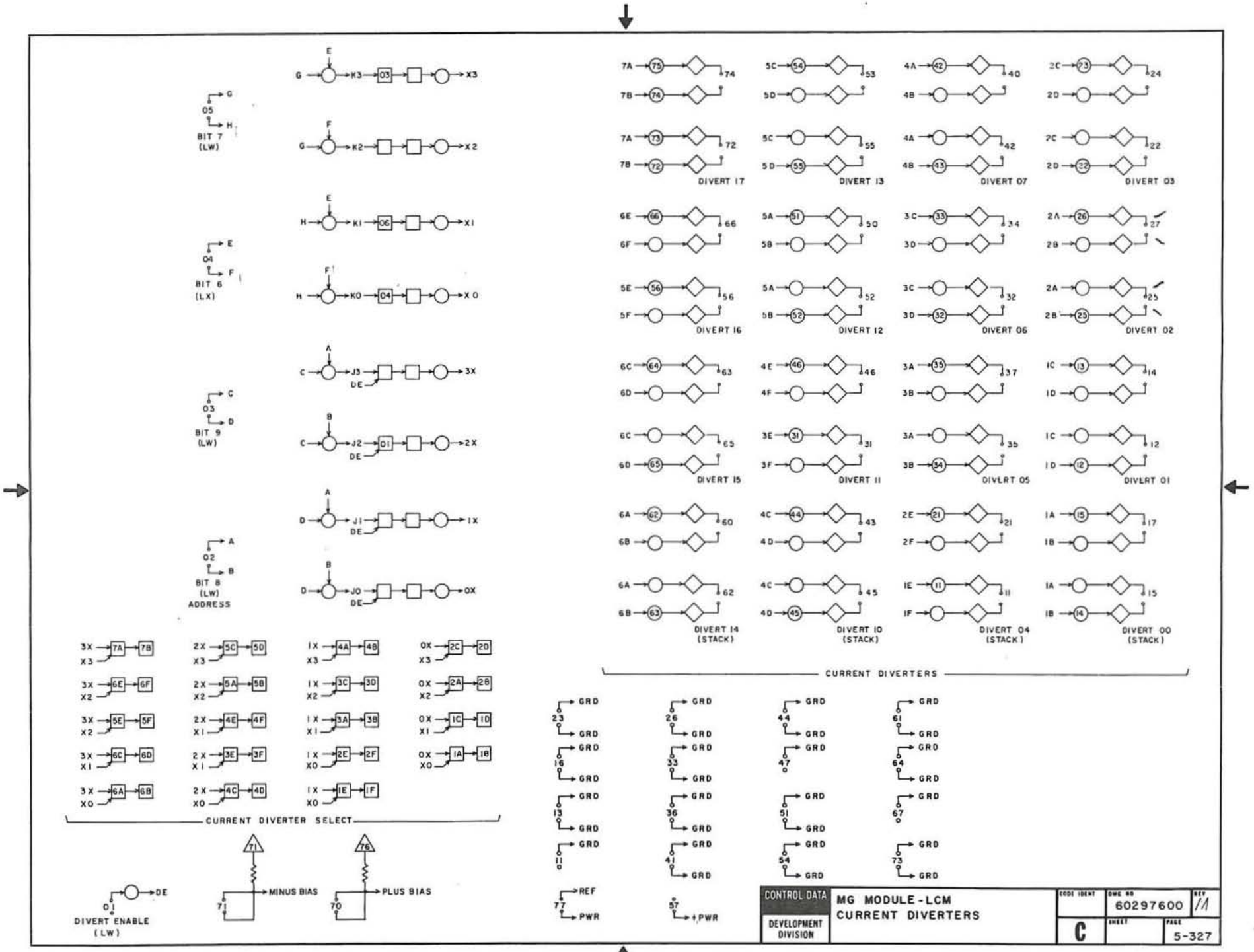
The MF module contains 32 Read/Write Current Drivers (transformers). Bits 10-14 of the LCM address determine which circuit is selected. The octal number assigned to each circuit is related to the binary value of the address bits. For example: if the address bits equal 10101, Read/Write 25 will be selected. Each circuit is connected to 16 read/write drive lines in one plane of an LCM stack. The selected circuit will apply read or write current to the drive lines. However, current will flow in only the line selected by a Current Diverter circuit (MG module). Direction of current flow is determined by either MF Module Read Enable or MF Module Write Enable signals. If neither of these signals is present, no current will flow. Only one of the 16 MF modules for the selected bank will receive these signals during the bank read/write cycle.



CONTROL DATA	MF MODULE - LCM READ/WRITE CURRENT DRIVERS	CODE IDENT	DWG NO 60297600	REV
DEVELOPMENT DIVISION		C	SHEET	PAGE 5-325

CURRENT DIVERTERS

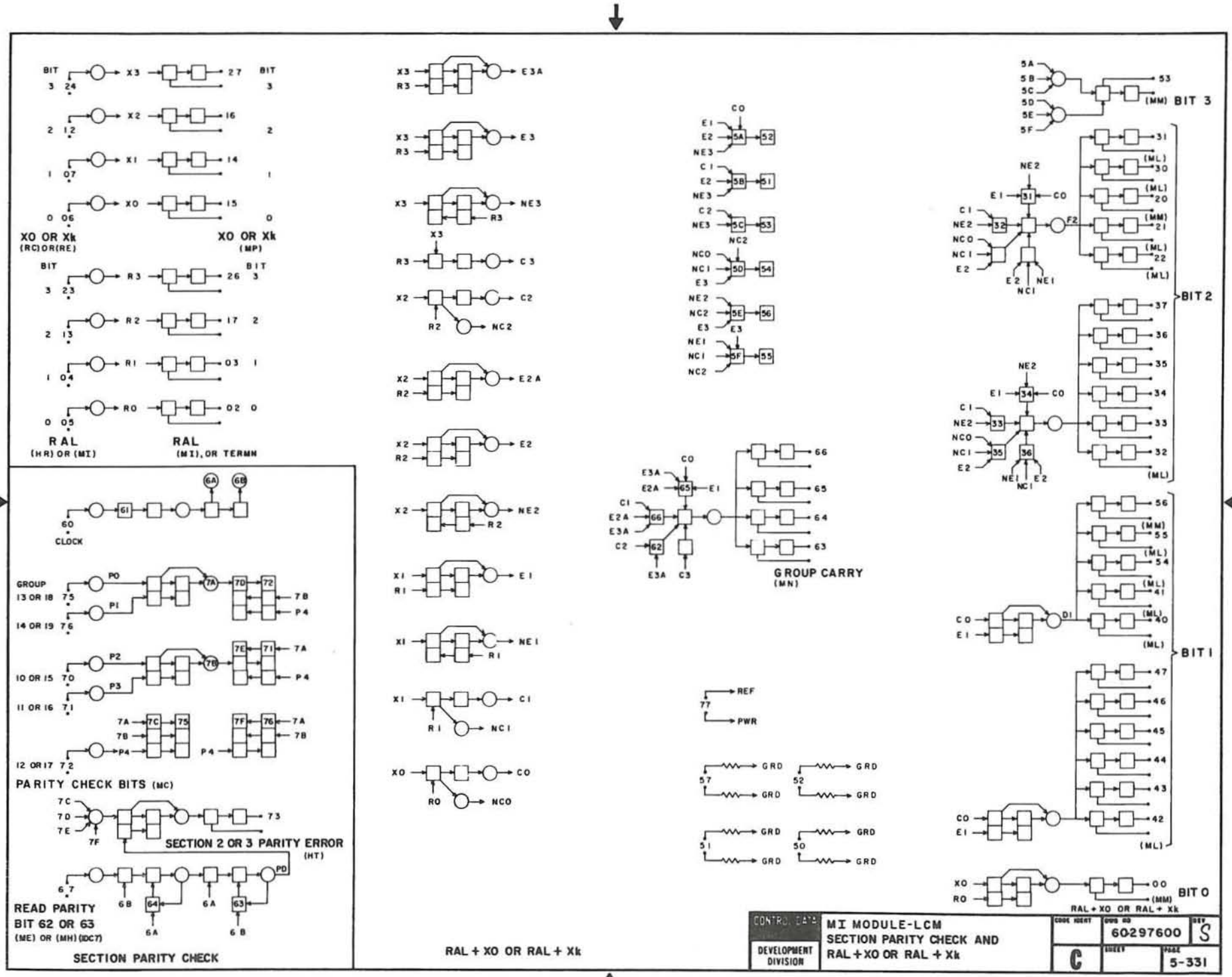
The MG module contains 16 pairs of Current Divert circuits. Bits 6-9 of the LCM address determine which pair is selected. The octal number assigned to each pair is related to the binary value of the address bits. For example: if the address bits equal 1010, Divert 12 will be selected. Each circuit is connected to two read/write drive lines on each of 16 planes in an LCM stack. When Divert Enable is present, the selected divert circuit completes a current path to ground. This allows current to flow thru one of 16 read/write drive lines in one plane that current is applied to by a selected Current Driver (MF module). The same divert circuit is selected in all eight MG modules for a selected bank. However; since each MG module is connected to different MF modules, current will flow thru only one drive line.

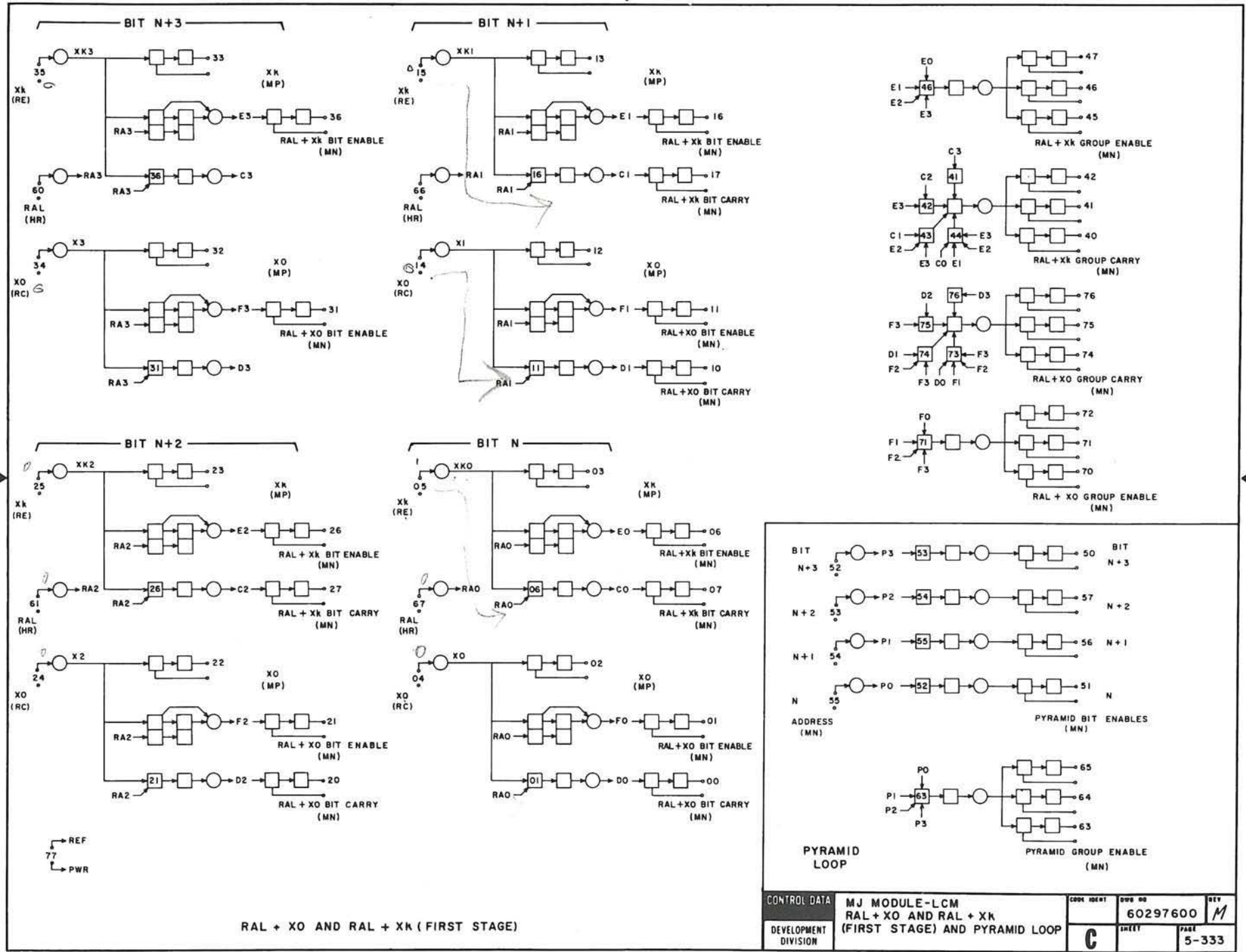

BIT 7 (LW)
BIT 6 (LX)
BIT 9 (LW)
BIT 8 (LW) ADDRESS
DE
DIVERT ENABLE (LW)
MINUS BIAS
PLUS BIAS
CURRENT DIVERTER SELECT
CURRENT DIVERTERS
DIVERT 17
DIVERT 13
DIVERT 07
DIVERT 03
DIVERT 16
DIVERT 12
DIVERT 06
DIVERT 02
DIVERT 15
DIVERT 11
DIVERT 05
DIVERT 01
DIVERT 14 (STACK)
DIVERT 10 (STACK)
DIVERT 04 (STACK)
DIVERT 00 (STACK)
GRD
REF
PWR
+PWR
CONTROL DATA
DEVELOPMENT DIVISION
MG MODULE-LCM
CURRENT DIVERTERS
60297600
REV 11
C
PAGE 5-327

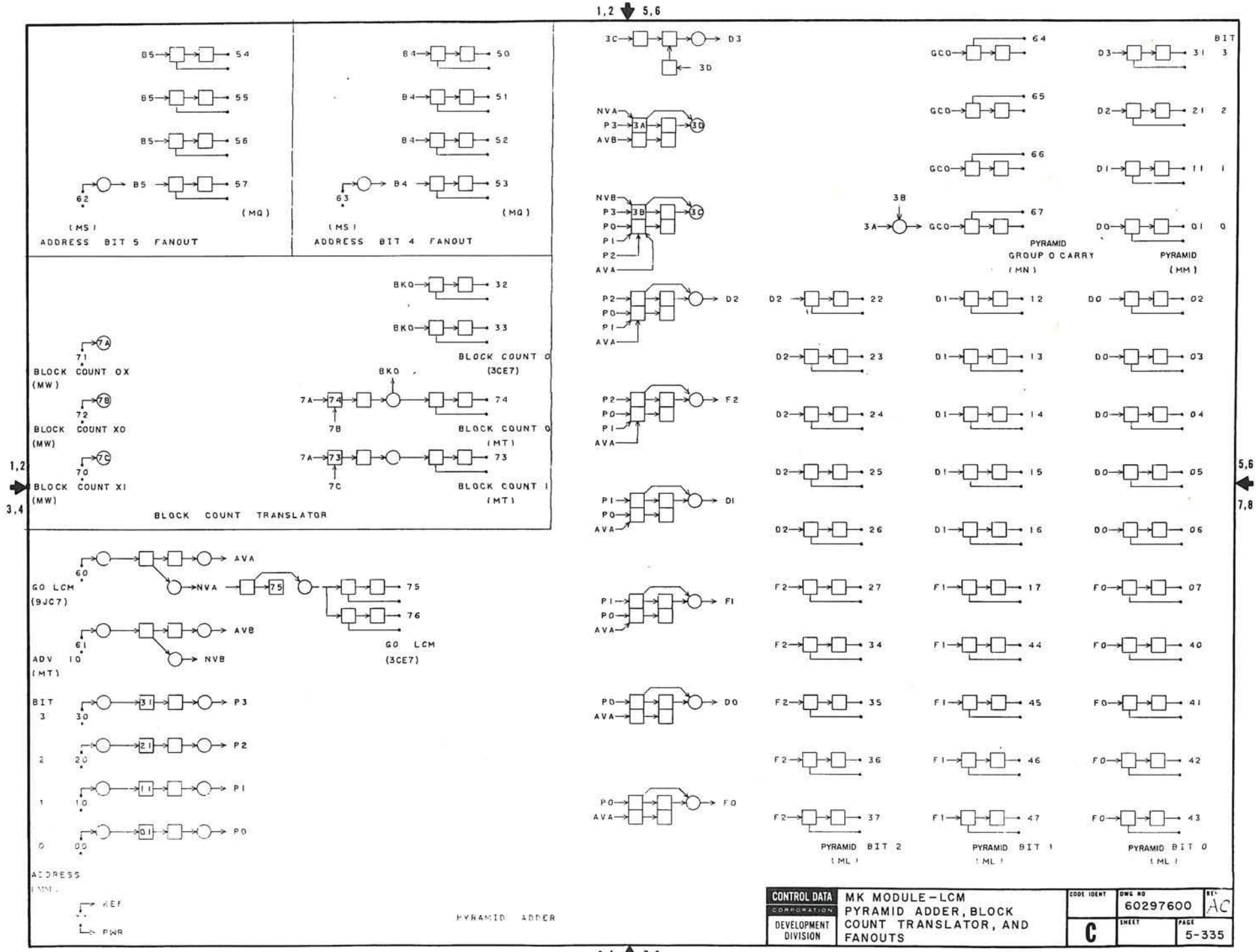
This page has been left blank intentionally. The MH module has been replaced by 1DC7 module.

SECTION PARITY CHECK

The MI module receives a Parity Check Bit from each of five Group Parity Check circuits (MC modules). The Section Parity Check circuit examines these bits. This circuit will send a Section Parity Error signal to the LCM Parity Error Register (HT module) if either of two conditions exist. These conditions are: odd number of Parity Check Bits are ones and Read Parity Bit is a one; or even number of Parity Check Bits are ones and Read Parity Bit is a zero.


XO OR Xk (RC) OR (RE)
XO OR Xk (MP)
RAL (HR) OR (MI)
RAL (MI), OR TERMN
CLOCK
GROUP 13 OR 18
14 OR 19
10 OR 15
11 OR 16
12 OR 17
PARITY CHECK BITS (MC)
SECTION 2 OR 3 PARITY ERROR (HT)
READ PARITY BIT 62 OR 63 (ME) OR (MH) (IDC7)
SECTION PARITY CHECK
RAL + XO OR RAL + Xk
GROUP CARRY (MN)
REF
PWR
GRD
BIT 3
BIT 2
BIT 1
BIT 0
(MM)
(ML)
RAL + XO OR RAL + Xk
CONTROL DATA
DEVELOPMENT DIVISION
MI MODULE-LCM
SECTION PARITY CHECK AND
RAL + XO OR RAL + Xk
60297600
S
C
5-331


BIT N+3
XK3
35
Xk (RE)
33
Xk (MP)
RA3
E3
36
RAL + Xk BIT ENABLE (MN)
60
RAL (HR)
C3
RAL + Xk BIT CARRY (MN)
X3
34
XO (RC)
32
XO (MP)
F3
31
RAL + XO BIT ENABLE (MN)
D3
RAL + XO BIT CARRY (MN)
BIT N+1
XK1
15
13
16
RAL + Xk BIT ENABLE (MN)
66
17
X1
14
12
11
10
BIT N+2
XK2
25
23
26
27
61
X2
24
22
21
20
BIT N
XKO
05
03
06
07
67
X0
04
02
01
00
REF
77
PWR
RAL + XO AND RAL + Xk (FIRST STAGE)
E0
E1
E2
46
47
45
RAL + Xk GROUP ENABLE (MN)
C3
C2
41
42
40
E3
43
44
C1
RAL + Xk GROUP CARRY (MN)
D2
76
D3
75
74
73
F3
F2
D1
RAL + XO GROUP CARRY (MN)
F0
F1
71
72
70
RAL + XO GROUP ENABLE (MN)
BIT N+3
52
P3
53
50
N+2
P2
54
57
N+1
P1
55
56
N
P0
52
51
55
ADDRESS (MN)
PYRAMID BIT ENABLES (MN)
PO
P1
P2
P3
63
65
64
PYRAMID GROUP ENABLE (MN)
PYRAMID LOOP
CONTROL DATA
DEVELOPMENT DIVISION
MJ MODULE-LCM
RAL + XO AND RAL + Xk
(FIRST STAGE) AND PYRAMID LOOP
CODE IDENT
C
DWG NO
60297600
REV
M
SHEET
PAGE
5-333


1,2
5,6
3,4
7,8
ADDRESS BIT 5 FANOUT
ADDRESS BIT 4 FANOUT
(MS)
(MQ)
BLOCK COUNT OX
(MW)
BLOCK COUNT XO
(MW)
BLOCK COUNT XI
(MW)
BLOCK COUNT TRANSLATOR
BLOCK COUNT 0
(3CE7)
BLOCK COUNT 0
(MT)
BLOCK COUNT 1
(MT)
GO LCM
(9JC7)
ADV 10
(MT)
GO LCM
(3CE7)
ADDRESS
(MM)
REF
PWR
PYRAMID ADDER
PYRAMID
GROUP 0 CARRY
(MN)
PYRAMID
(MM)
BIT
PYRAMID BIT 2
(ML)
PYRAMID BIT 1
(ML)
PYRAMID BIT 0
(ML)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
MK MODULE-LCM
PYRAMID ADDER, BLOCK COUNT TRANSLATOR, AND FANOUTS
CODE IDENT
C
DWG NO
60297600
REV
AC
SHEET
PAGE
5-335

ADDRESS SELECTION

Address bits 1 and 2 enter the holding register every clock period from one of three sources. These are RAL + Xk, RAL + K0 and Pyramid. The selection is based on the condition of Enter Xk, Enter X0, and Pyramid Bit 0. These two address bits are fanned out to the MB modules.

RAL + Xk

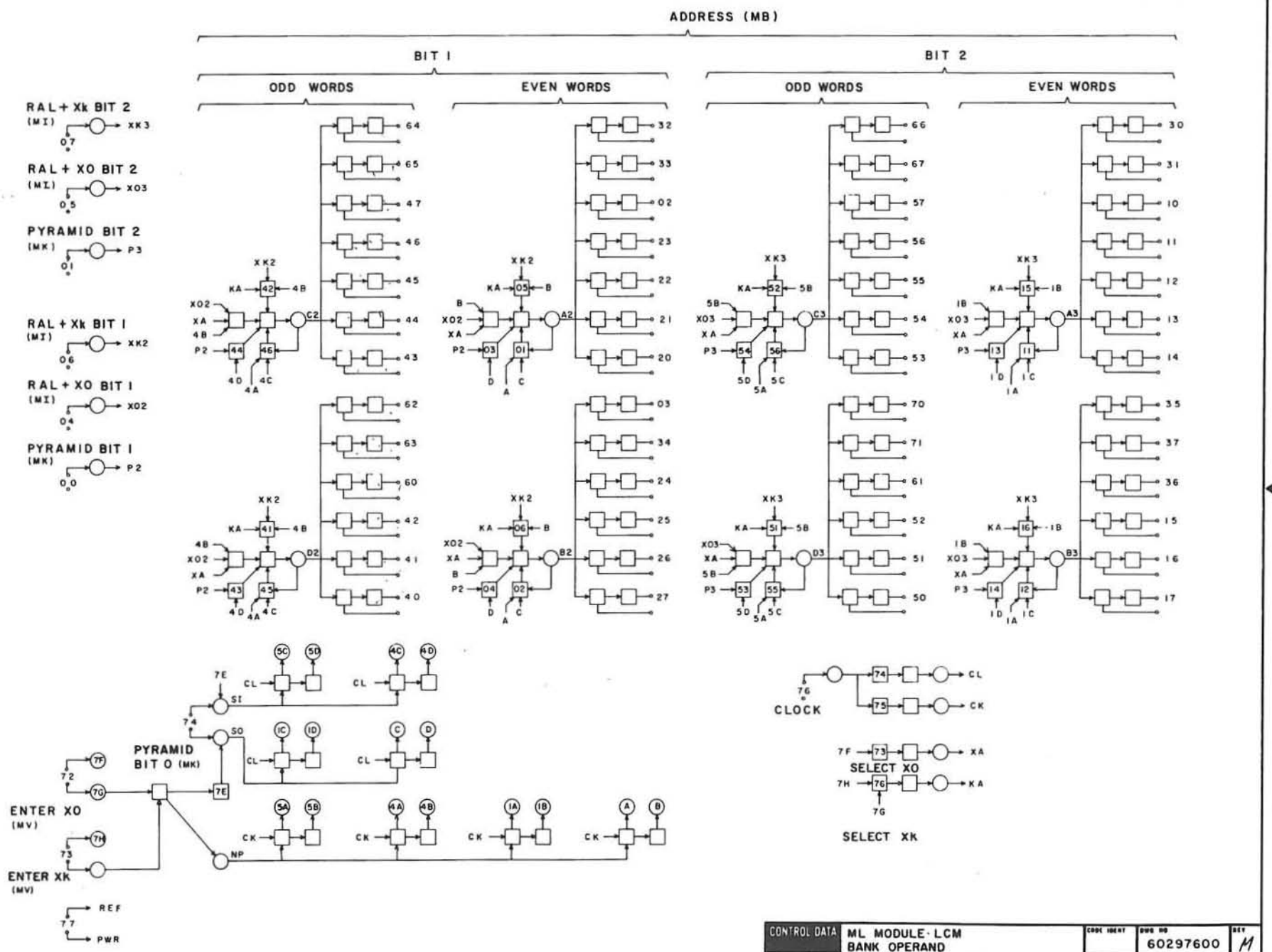
RAL + Xk Bits 1 and 2 enter odd and even word sections when Enter Xk is present and Enter X0 is absent.

RAL + X0

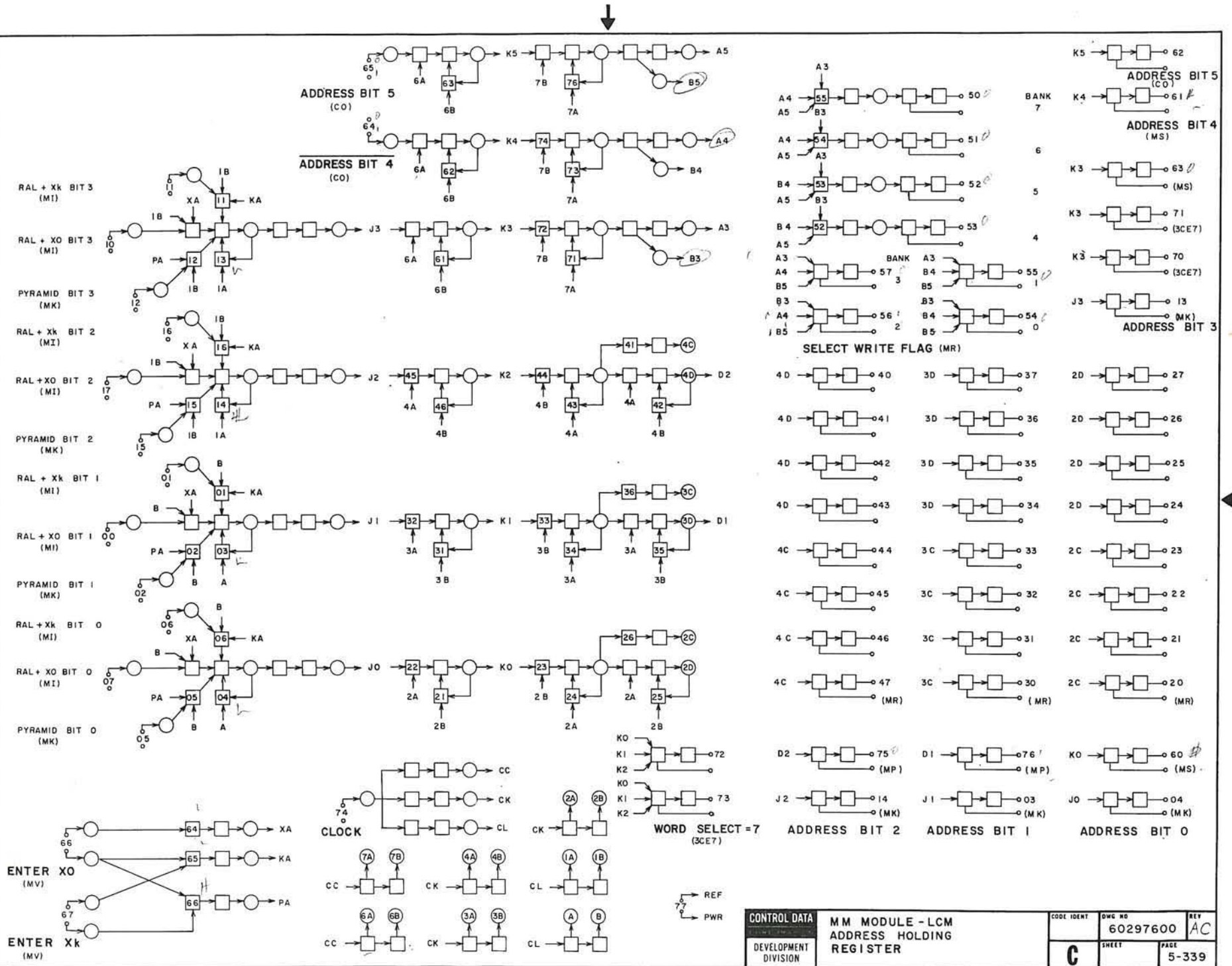
RAL + X0 Bits 1 and 2 enter odd and even word sections when Enter X0 is present.

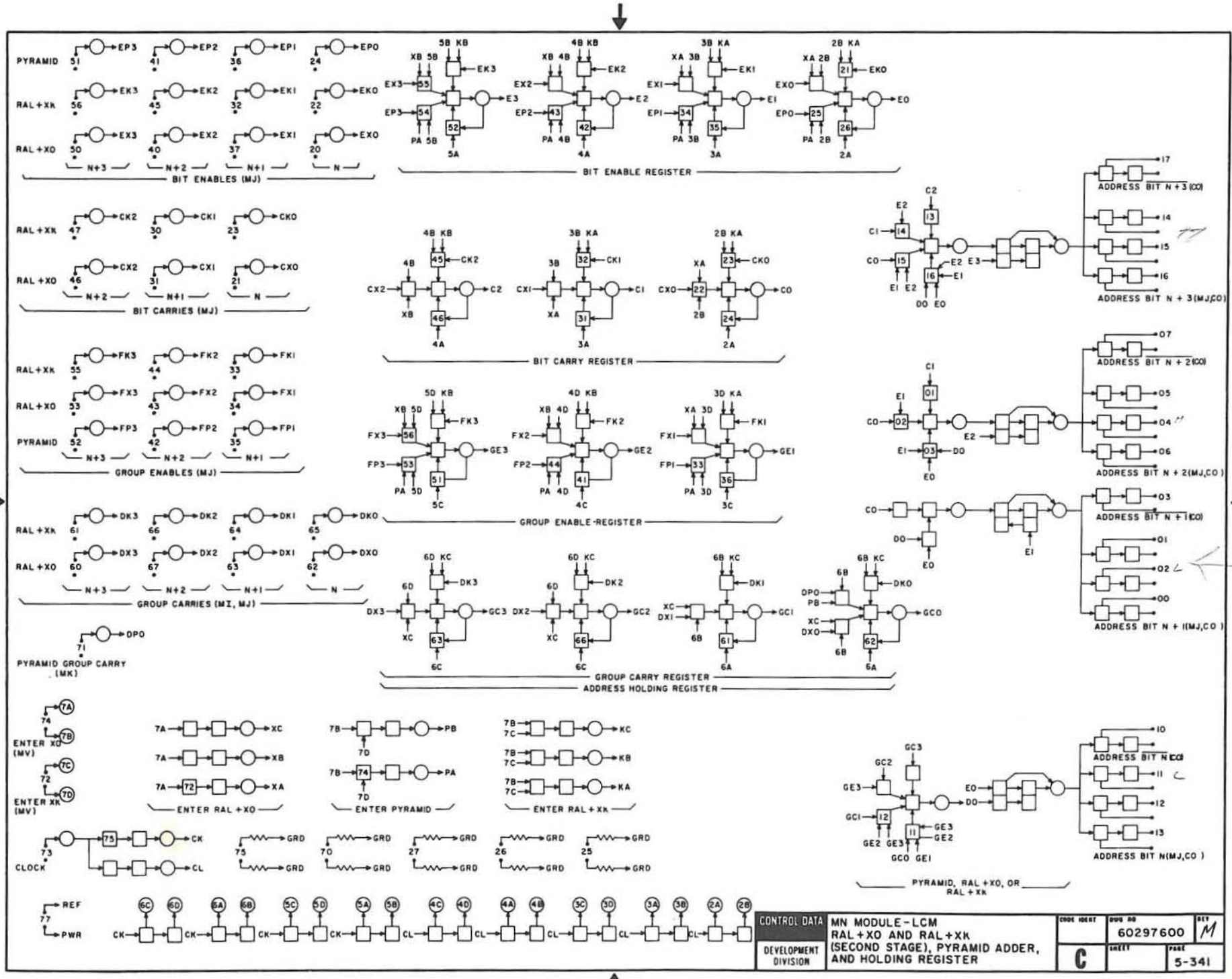
PYRAMID

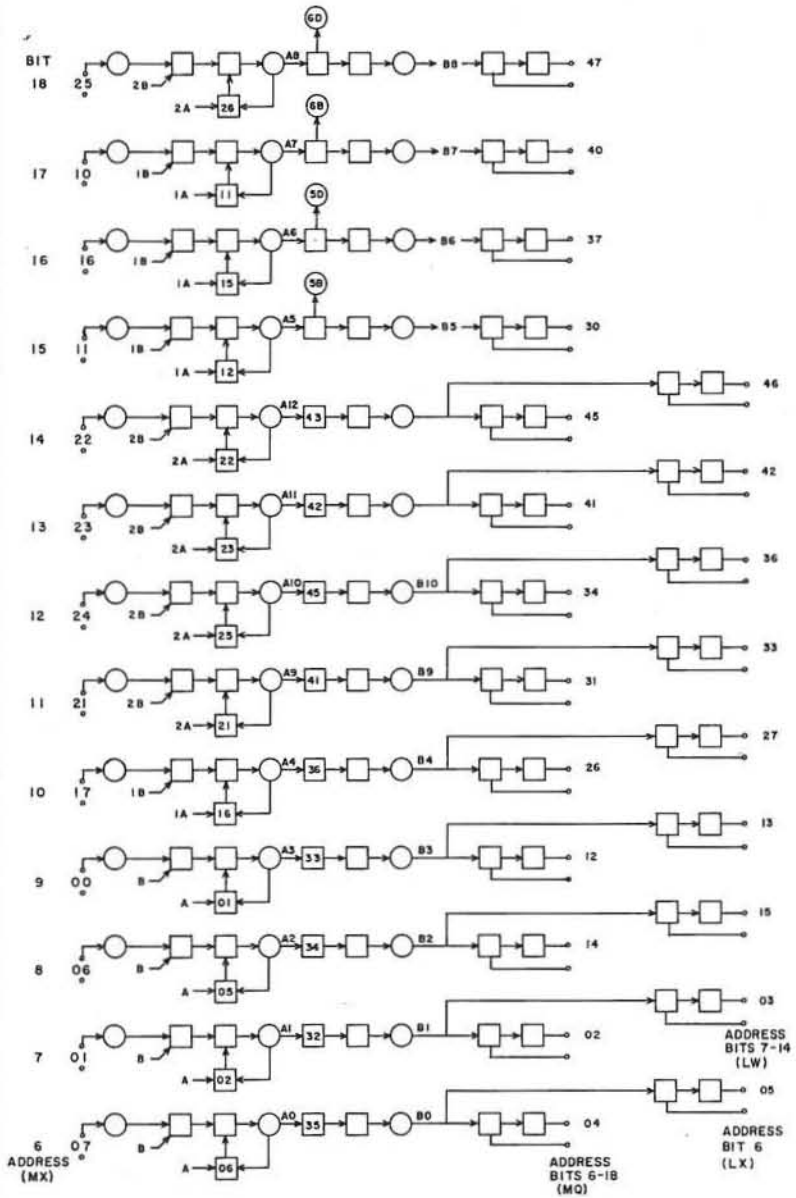
Pyramid Bits 1 and 2 enter the odd word section when Enter Xk and Enter X0 are absent and Pyramid Bit 0 is a one. They enter the even bank section when Enter Xk and Enter X0 are absent and Pyramid Bit 0 is a zero.



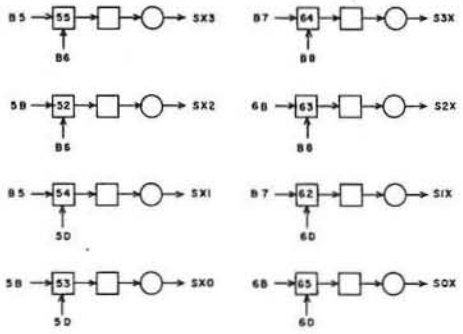
CONTROL DATA	ML MODULE-LCM BANK OPERAND REGISTER READ SELECT AND FANOUT	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	M
			SHEET	PAGE 5-337


ADDRESS BIT 5
(CO)
ADDRESS BIT 4
(CO)
RAL + Xk BIT 3
(MI)
RAL + XO BIT 3
(MI)
PYRAMID BIT 3
(MK)
RAL + Xk BIT 2
(MI)
RAL + XO BIT 2
(MI)
PYRAMID BIT 2
(MK)
RAL + Xk BIT 1
(MI)
RAL + XO BIT 1
(MI)
PYRAMID BIT 1
(MK)
RAL + Xk BIT 0
(MI)
RAL + XO BIT 0
(MI)
PYRAMID BIT 0
(MK)
ENTER XO
(MV)
ENTER Xk
(MV)
CLOCK
WORD SELECT = 7
(3CE7)
REF
PWR
SELECT WRITE FLAG (MR)
BANK
ADDRESS BIT 5
ADDRESS BIT 4
(MS)
ADDRESS BIT 3
(MK)
ADDRESS BIT 2
ADDRESS BIT 1
ADDRESS BIT 0
CONTROL DATA
DEVELOPMENT DIVISION
MM MODULE - LCM
ADDRESS HOLDING
REGISTER
CODE IDENT
DWG NO
60297600
REV
AC
C
SHEET
PAGE
5-339

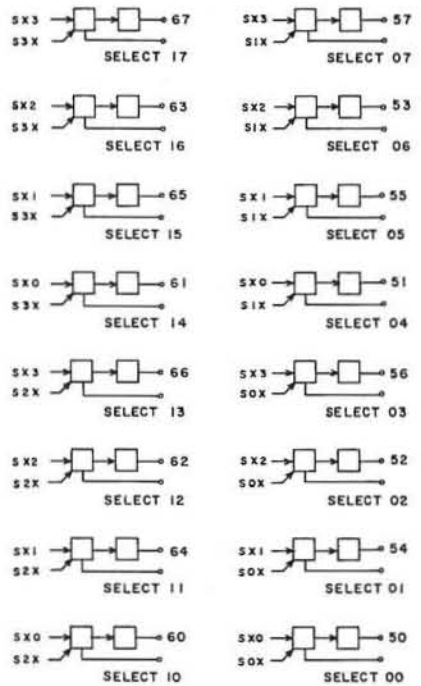

PYRAMID
RAL+XK
RAL+XO
BIT ENABLES (MJ)
BIT ENABLE REGISTER
BIT CARRIES (MJ)
BIT CARRY REGISTER
GROUP ENABLES (MJ)
GROUP ENABLE REGISTER
GROUP CARRIES (MI, MJ)
GROUP CARRY REGISTER
ADDRESS HOLDING REGISTER
PYRAMID GROUP CARRY (MX)
ENTER XO (MV)
ENTER XK (MV)
ENTER RAL+XO
ENTER PYRAMID
ENTER RAL+XK
CLOCK
ADDRESS BIT N+3 (CO)
ADDRESS BIT N+3 (MJ,CO)
ADDRESS BIT N+2 (CO)
ADDRESS BIT N+2 (MJ,CO)
ADDRESS BIT N+1 (CO)
ADDRESS BIT N+1 (MJ,CO)
ADDRESS BIT N (CO)
ADDRESS BIT N (MJ,CO)
PYRAMID, RAL+XO, OR RAL+XK
CONTROL DATA
DEVELOPMENT DIVISION
MN MODULE - LCM
RAL+XO AND RAL+XK
(SECOND STAGE), PYRAMID ADDER,
AND HOLDING REGISTER
CODE IDENT
C
DWG NO
60297600
REV
M
SHEET
PAGE
5-341



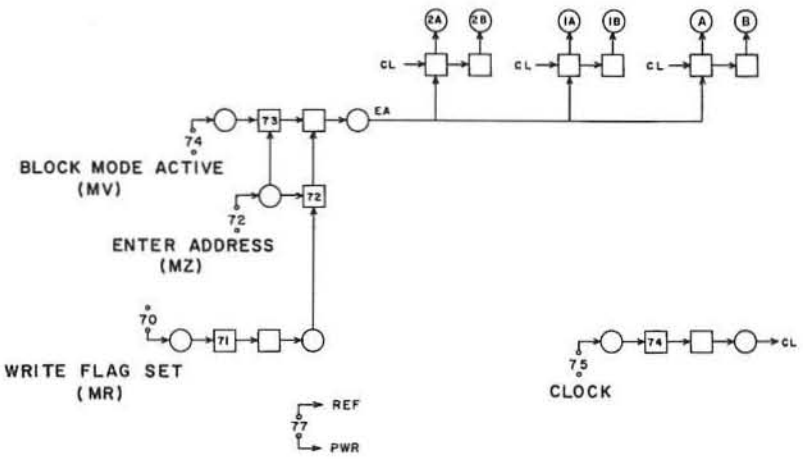
BANK ADDRESS REGISTER



MF MODULE SELECT



SELECTED MF MODULE (LX)



CONTROL DATA DEVELOPMENT DIVISION	MO MODULE - LCM BANK ADDRESS REGISTER AND MF MODULE SELECT	CODE IDENT C	DWG NO 60297600 SHEET	REV AD PAGE 5-343

ADDRESS RANGE TEST

Two MP modules perform a partial arithmetic computation on three operands. Operand B (BX terms) is added to operand C (CX terms). This sum is subtracted from operand A (AX terms). A check is made in an MQ module to determine if operand A is equal to or greater than the sum of operands B and C. This check is based on Group Borrows and Enables generated by the MP modules. If operand A is less than the sum of operands B and C, one of the following signal combinations will be generated: Group 3 Borrow, Group 2 Borrow and Group 3 Enable, Group 1 Borrow and Group 2 and 3 Enable, or Group 0 Borrow and Groups 1-3 Enable.

The following chart shows what occurs in a single MP module when three arbitrary operands are applied. The AX terms are the complement of operand A which is 0100101001. The BX terms are operand B which is 0010111011. The CX terms are operand C which is 0100010101.

Terms	Group 1 Bits					Group 0 Bits					Operation
	9	8	7	6	5	4	3	2	1	0	
B9-B0	0	0	1	0	1	1	1	0	1	1	
C9-C0	0	1	0	0	0	1	0	1	0	1	
4B-1A	0	1	1	0	1	0	1	1	1	0	EXCLUSIVE OR
A9-A0	1	0	1	1	0	1	0	1	1	0	
4D-1C	1	1	0	1	1	1	1	0	0	0	EXCLUSIVE OR
BI9-B10	0	1	0	0	1	0	1	1	1	0	AND-OR (Note 1)
E9-E0	1	0	0	1	0	1	0	0	1	0	EXCLUSIVE OR (Note 2)
D9-D0	0	1	0	0	1	0	1	0	0	0	AND (Note 3)
7G-6C	1	0	1	1	1	1	0	1	1	1	NOT-OR (Note 4)

NOTES

1. BI0 = "0", BI1=B0 · C0+A0 1A, BI2=B1 · C1+A1 · 1B, etc.
2. E23 = E3 (2C · $\overline{BI2}$+$\overline{2C}$ · BI2), E89 = E9 (4C · $\overline{BI8}$+$\overline{4C}$ · BI8)
3. D0 = 1C · BI0, D1 = 1D · BI1, etc.
4. 6C = $\overline{D0}$+$\overline{E1}$+$\overline{E4}$+$\overline{E23}$, 6D = $\overline{D1}$+$\overline{E23}$+$\overline{E4}$, 6E = $\overline{D2}$+$\overline{E3}$+$\overline{E4}$, 6F = $\overline{D3}$+$\overline{E4}$, 6G = $\overline{D4}$, 7C = $\overline{D5}$+$\overline{E6}$+$\overline{E7}$+$\overline{E89}$, 7D = $\overline{D6}$+$\overline{E7}$+$\overline{E89}$, 7E = $\overline{D7}$+$\overline{E89}$, 7F = $\overline{D8}$+$\overline{E9}$, 7G = $\overline{D9}$

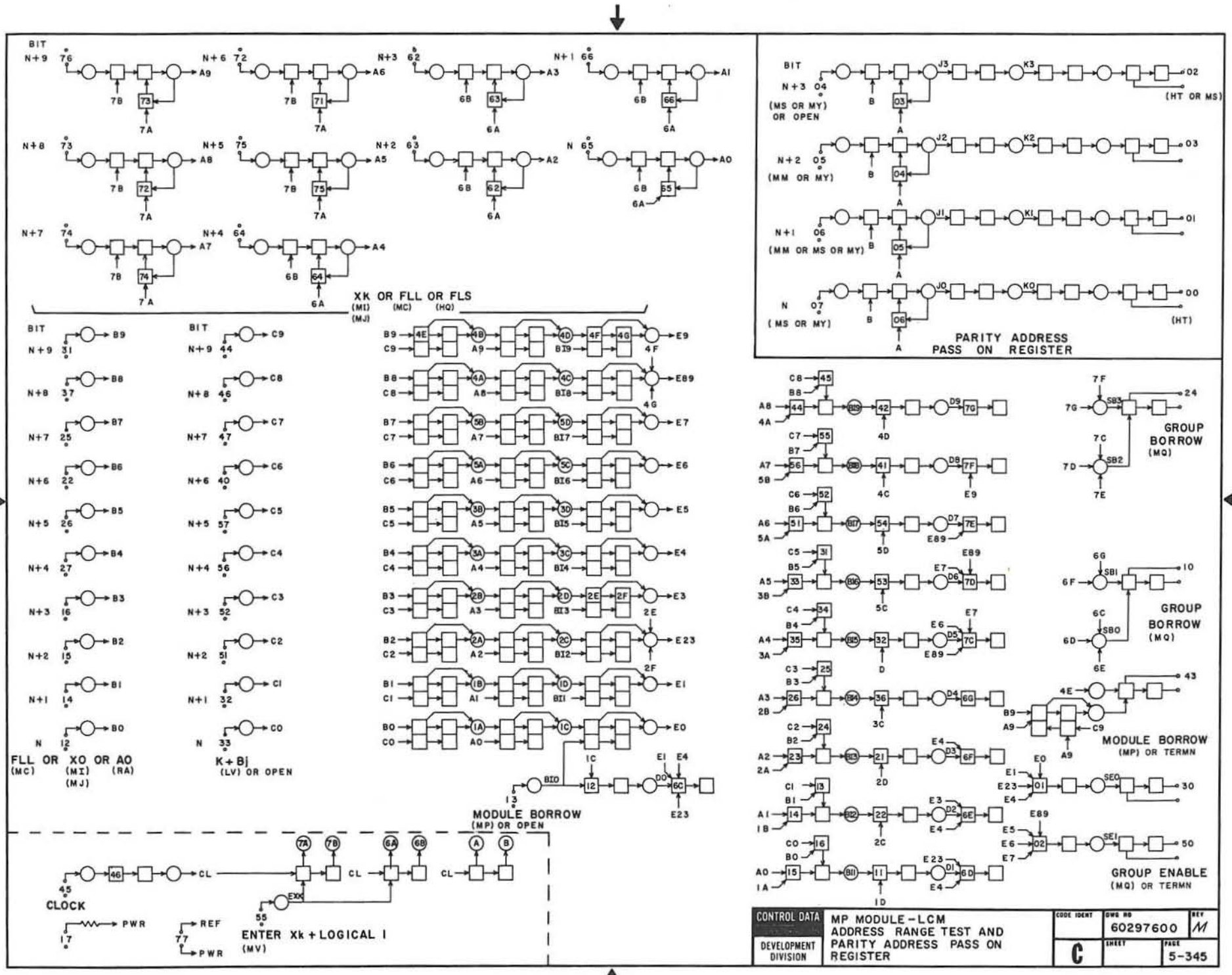
The Module Borrow output will not be generated when these three operands are used. This output will be generated when any one of the following conditions exist: A9 · B9 · C9+A9 · B9 · $\overline{C9}$+A9 · $\overline{B9}$ · C9+A9 · $\overline{B9}$ · $\overline{C9}$.

The Group 0 Borrow output will be generated because the 6F term is a zero. This output will be generated when anyone of the following conditions exist: $\overline{6C}$+$\overline{6D}$+$\overline{6E}$+$\overline{6F}$+$\overline{6G}$.

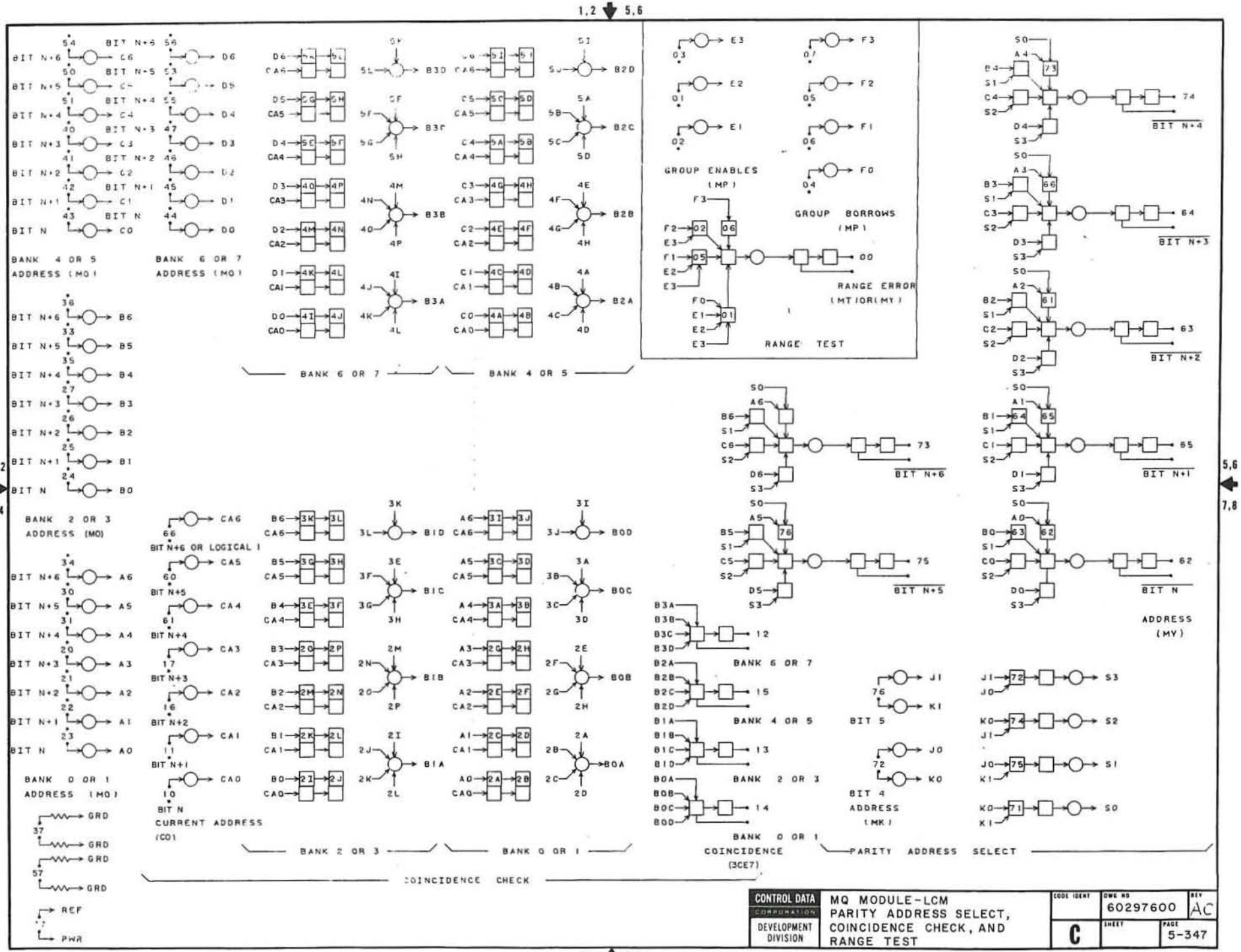
The Group 0 Enable output will not be generated because the E0 and E2 terms are zeros. This output will be generated when the following condition exists: E0 · E1 · E23 · E4.

The Group 1 Borrow output will be generated because the 7F term is a zero. This output will be generated when any one of the following conditions exist: $\overline{7C}$+$\overline{7D}$+$\overline{7E}$+$\overline{7F}$+$\overline{7G}$.

The Group 1 Enable output will not be generated because the E5, E7, and E89 terms are zeros. This output will be generated when the following conditions exists: E5 · E6 · E7 · E89.



CONTROL DATA	MP MODULE - LCM ADDRESS RANGE TEST AND PARITY ADDRESS PASS ON REGISTER	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	M
			SHEET	PAGE 5-345


1,2
5,6
3,4
7,8
BIT N+6
BIT N+5
BIT N+4
BIT N+3
BIT N+2
BIT N+1
BIT N
BANK 4 OR 5 ADDRESS (MO)
BANK 6 OR 7 ADDRESS (MO)
BANK 2 OR 3 ADDRESS (MO)
BANK 0 OR 1 ADDRESS (MO)
BIT N CURRENT ADDRESS (CO)
GRD
REF
PWR
BANK 6 OR 7
BANK 4 OR 5
BANK 2 OR 3
BANK 0 OR 1
COINCIDENCE CHECK
GROUP ENABLES (MP)
GROUP BORROWS (MP)
RANGE ERROR (MTIOR(MY)
RANGE TEST
BIT N+6 OR LOGICAL 1
BANK 6 OR 7
BANK 4 OR 5
BANK 2 OR 3
BANK 0 OR 1
COINCIDENCE (3CE7)
BIT 5
BIT 4 ADDRESS (MK)
PARITY ADDRESS SELECT
ADDRESS (MY)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
MQ MODULE-LCM
PARITY ADDRESS SELECT, COINCIDENCE CHECK, AND RANGE TEST
CODE IDENT C
DWG NO 60297600
REV AC
SHEET
PAGE 5-347

BANK WRITE/SENSE CONTROL

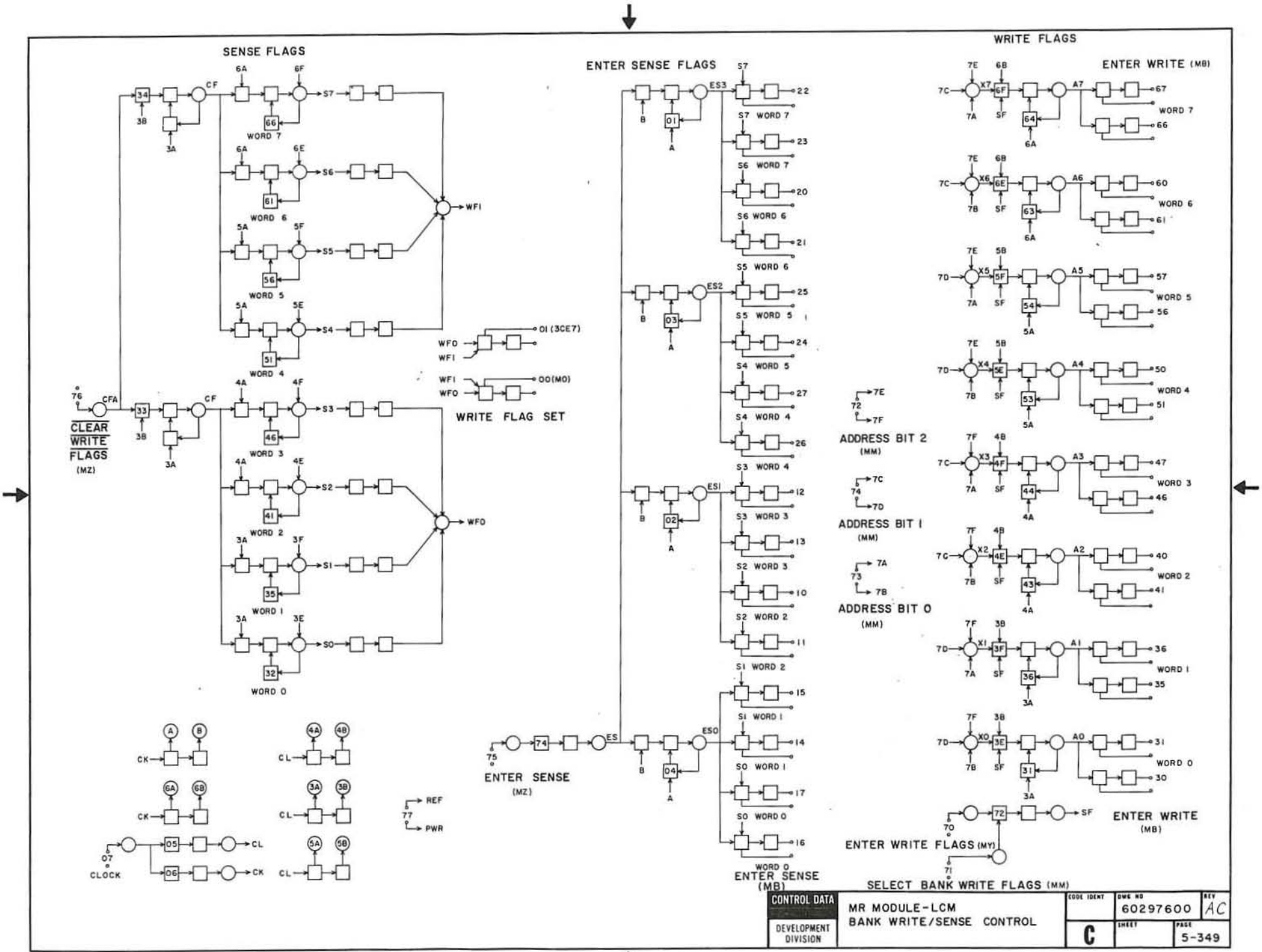
The MR module is used to control the entry of data into a Bank Operand Register (MB modules). Either complemented sense or write data will enter this register. The data paths are dependent on the condition of control flags. Data enters the word sections of the register for which the corresponding Words 0-7 Sense Flags or Write Flags are set.

WORDS 0-7 SENSE FLAGS

All Sense Flags are set simultaneously during a clock period in which a Clear Write Flags signal is not present. However; if any of the Write Flags are being set (any 3E-6F term a zero) at the same time, the corresponding Sense Flag will not be set. The Sense Flags are cleared individually when the corresponding Write Flags are set. When any of the Sense Flags is clear (any S0-S7 term a zero), a Write Flag Set signal will be generated. Words 0-7 Enter Sense signals are sent to the Bank Operand Register during a clock period in which the corresponding Sense Flags are set and Enter Sense is present.

WORDS 0-7 WRITE FLAGS

One of eight Write Flags will be cleared and set during a clock period in which Enter Write Flags and Select Bank (X) Write Flags signals are present. The individual Write Flags are selected based on the condition of Address Bits 0-2. Words 0-7 Enter Write signals are sent to the Bank Operand Register during the clock period that the corresponding Write Flags are set.


SENSE FLAGS
ENTER SENSE FLAGS
WRITE FLAGS
ENTER WRITE (MB)
CLEAR WRITE FLAGS (MZ)
WRITE FLAG SET
ENTER SENSE (MZ)
ENTER SENSE (MB)
ENTER WRITE FLAGS (MY)
ENTER WRITE (MB)
ADDRESS BIT 2 (MM)
ADDRESS BIT 1 (MM)
ADDRESS BIT 0 (MM)
SELECT BANK WRITE FLAGS (MM)
CLOCK
WORD 7
WORD 6
WORD 5
WORD 4
WORD 3
WORD 2
WORD 1
WORD 0
WFI
WFO
CONTROL DATA
DEVELOPMENT DIVISION
MR MODULE-LCM
BANK WRITE/SENSE CONTROL
60297600
AC
C
5-349

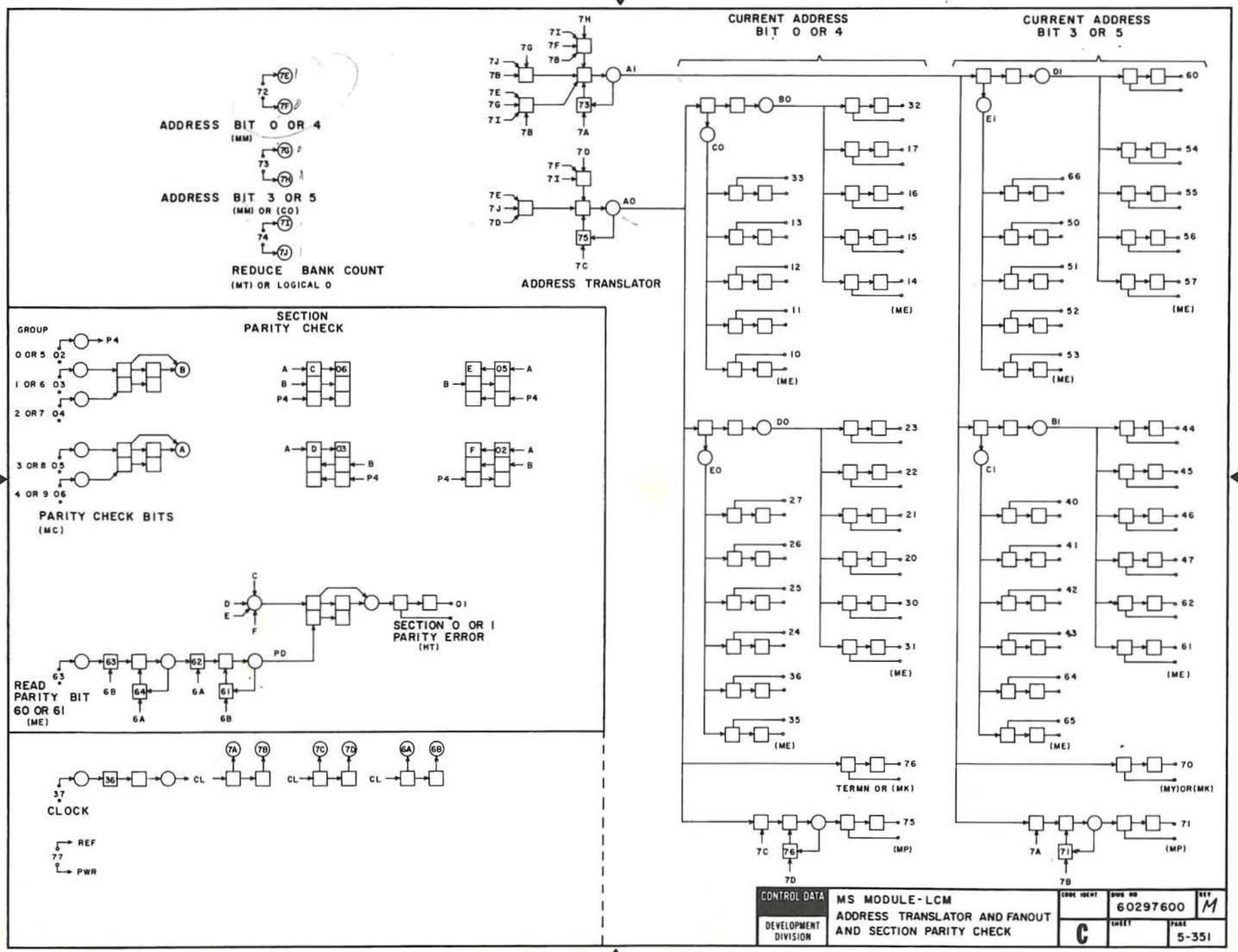
SECTION PARITY CHECK

The MS module receives a Parity Check Bit from each of five Group Parity Check circuits (MC modules). The Section Parity Check circuit examines these bits. This circuit will send a Section Parity Error signal to the LCM Parity Error Register (HT module) if either of two conditions exist. These conditions are: odd number of Parity Check Bits are ones and Read Parity Bit is a one; or even number of Parity Check Bits are ones and Read Parity Bit is a zero.

ADDRESS TRANSLATOR

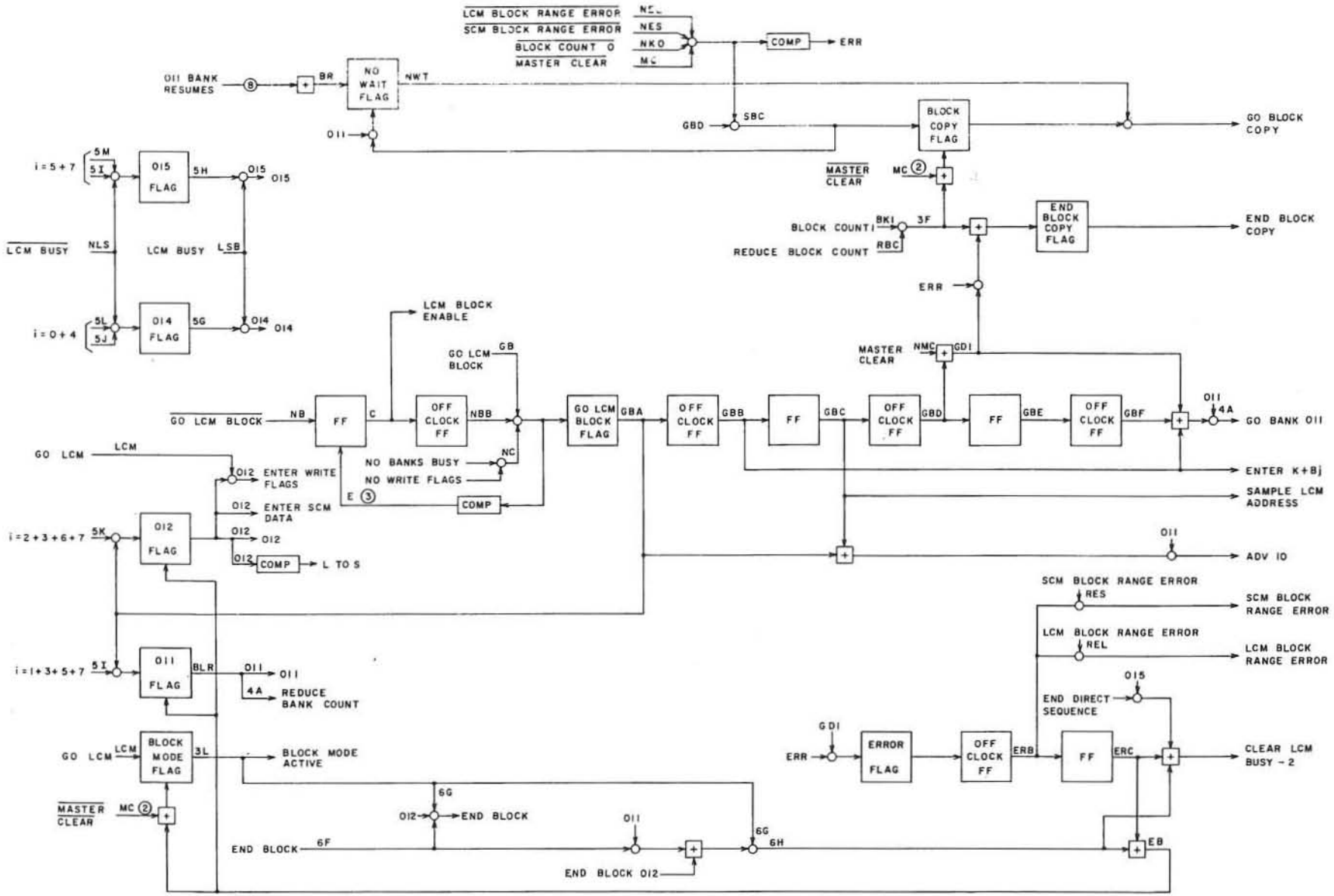
Two MS modules are used to reduce the octal value of Address Bits 3-5 by two when Reduce Bank Count (RBC) is present. RBC is present only when an 011 instruction is executed. If RBC is not present the bits are unchanged. A logical zero is substituted for RBC in the module that translates bits 0 and 3. When RBC is present: bit 4 is complemented, bit 5 is complemented if bit 4 was a zero and unchanged if bit 4 was a one, bit 3 is unchanged, and bit 0 is unchanged. The eight possible translations are as follows:

Input				Output			
5	4	3		5	4	3	
0	0	0	(0)	1	1	0	(6)
0	0	1	(1)	1	1	1	(7)
0	1	0	(2)	0	0	0	(0)
0	1	1	(3)	0	0	1	(1)
1	0	0	(4)	0	1	0	(2)
1	0	1	(5)	0	1	1	(3)
1	1	0	(6)	1	0	0	(4)
1	1	1	(7)	1	0	1	(5)



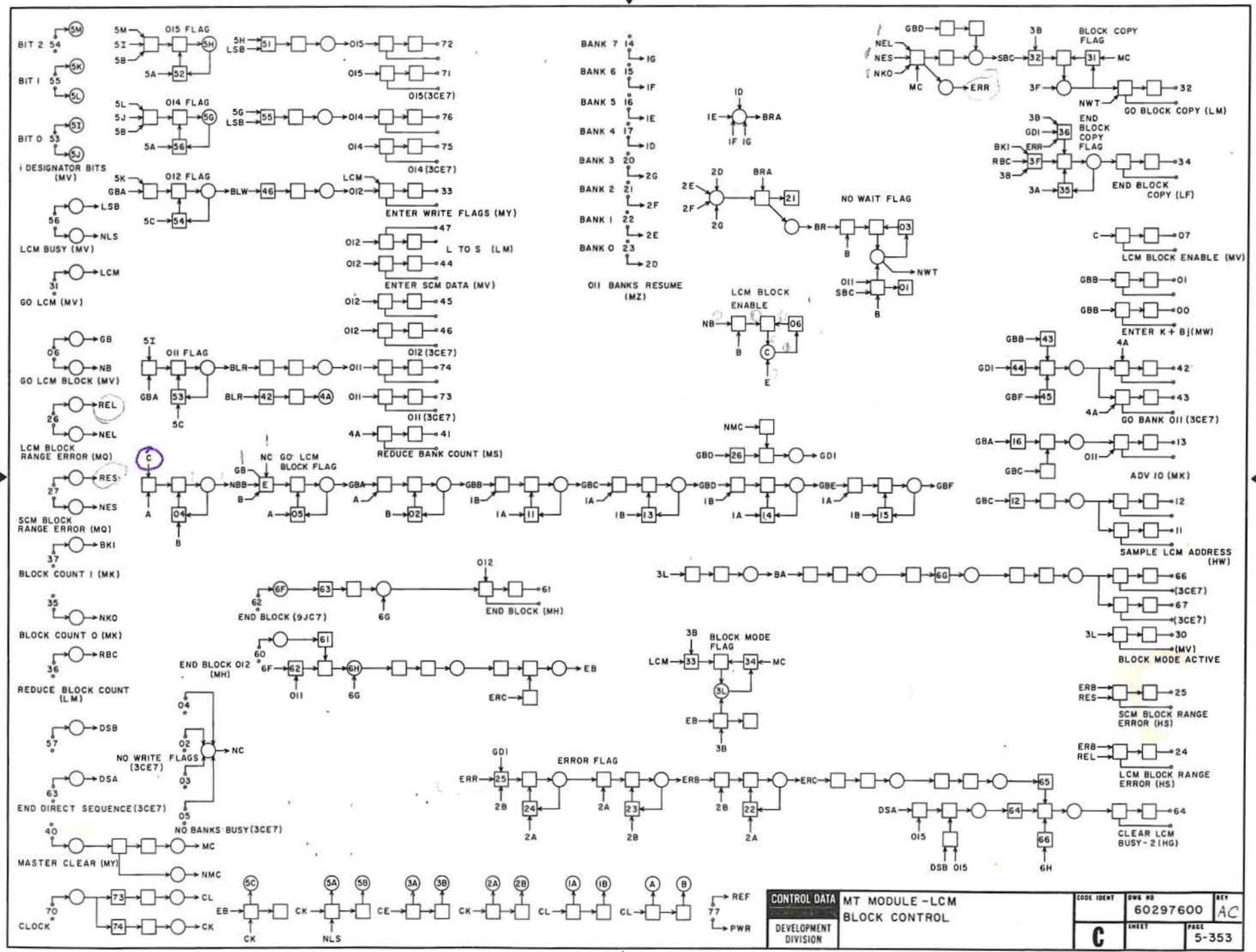
CONTROL DATA	MS MODULE-LCM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	ADDRESS TRANSLATOR AND FANOUT AND SECTION PARITY CHECK	C	60297600	M
		SHEET	PAGE 5-351	

MT MODULE BLOCK DIAGRAM

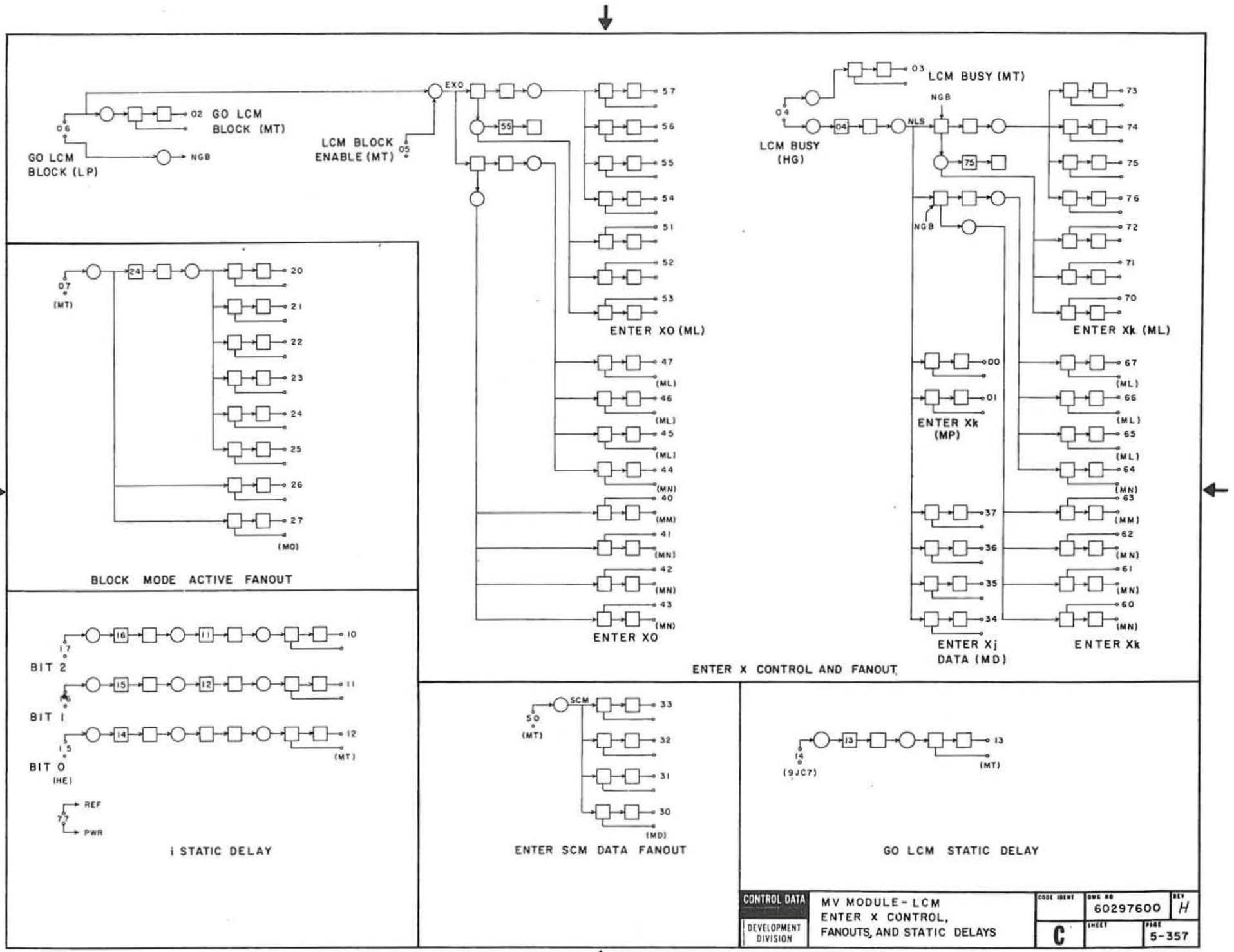


NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL SETTING, CLEARING, AND GATING TERMS ARE ONES.
2. MASTER CLEAR INPUT MAKES MC TERM A ZERO, WHICH CLEARS FLAG.
3. FF CLEARS WHEN E TERM IS A ZERO.


BIT 2 54
BIT 1 55
BIT 0 53
I DESIGNATOR BITS (MV)
LCM BUSY (MV)
GO LCM (MV)
GO LCM BLOCK (MV)
LCM BLOCK RANGE ERROR (MQ)
SCM BLOCK RANGE ERROR (MQ)
BLOCK COUNT 1 (MK)
BLOCK COUNT 0 (MK)
REDUCE BLOCK COUNT (LM)
END DIRECT SEQUENCE (3CE7)
MASTER CLEAR (MY)
CLOCK
O15 FLAG
O14 FLAG
O12 FLAG
O11 FLAG
ENTER WRITE FLAGS (MY)
L TO S (LM)
ENTER SCM DATA (MV)
O12 (3CE7)
O11 (3CE7)
REDUCE BANK COUNT (MS)
NC GO LCM BLOCK FLAG
NO WRITE FLAGS (3CE7)
NO BANKS BUSY (3CE7)
END BLOCK (9JC7)
END BLOCK (MH)
END BLOCK O12 (MH)
BANK 7
BANK 6
BANK 5
BANK 4
BANK 3
BANK 2
BANK 1
BANK 0
O11 BANKS RESUME (MZ)
NO WAIT FLAG
LCM BLOCK ENABLE
BLOCK COPY FLAG
END BLOCK COPY FLAG
GO BLOCK COPY (LM)
END BLOCK COPY (LF)
LCM BLOCK ENABLE (MV)
ENTER K + BJ (MW)
GO BANK O11 (3CE7)
ADV 10 (MK)
SAMPLE LCM ADDRESS (HW)
BLOCK MODE FLAG
BLOCK MODE ACTIVE
SCM BLOCK RANGE ERROR (HS)
LCM BLOCK RANGE ERROR (HS)
ERROR FLAG
CLEAR LCM BUSY - 2 (HG)
CONTROL DATA
DEVELOPMENT DIVISION
MT MODULE - LCM
BLOCK CONTROL
CODE IDENT
DWG NO
60297600
REV
AC
SHEET
C
PAGE
5-353

This page has been left blank intentionally. The
MU module has been replaced by the 1CE7 module.


GO LCM BLOCK (LP)
06
02 GO LCM BLOCK (MT)
NGB
LCM BLOCK ENABLE (MT)
05
EX0
55
57
56
55
54
51
52
53
ENTER X0 (ML)
47 (ML)
46 (ML)
45 (ML)
44 (MN)
40 (MM)
41 (MN)
42 (MN)
43 (MN)
ENTER X0
03
LCM BUSY (MT)
04
LCM BUSY (HG)
NGB
NLS
04
75
NGB
73
74
75
76
72
71
70
ENTER Xk (ML)
00
01
ENTER Xk (MP)
67 (ML)
66 (ML)
65 (ML)
64 (MN)
63 (MM)
62 (MN)
61 (MN)
60 (MN)
ENTER Xk
37
36
35
34
ENTER Xj DATA (MD)
ENTER X CONTROL AND FANOUT
07 (MT)
24
20
21
22
23
24
25
26
27 (MO)
BLOCK MODE ACTIVE FANOUT
17
BIT 2
16
11
10
16
BIT 1
15
12
11
15
BIT 0 (HE)
14
12 (MT)
REF
77
PWR
i STATIC DELAY
SCM
50 (MT)
33
32
31
30 (MD)
ENTER SCM DATA FANOUT
14 (9JC7)
13
13 (MT)
GO LCM STATIC DELAY
CONTROL DATA
DEVELOPMENT DIVISION
MV MODULE - LCM
ENTER X CONTROL,
FANOUTS, AND STATIC DELAYS
CODE IDENT
C
DWG NO
60297600
REV
H
SHEET
PAGE
5-357

BLOCK COUNT REGISTER AND REDUCER

Two MW modules and a MK module are used to determine when the block count is reduced to one, and then to zero. The total number of words (block count) in a block copy is the octal value of K + Bj bits 0-9. This block count is reduced by one each clock period during a block copy instruction. One MW module contains the Block Count Register, Block Count Check, and Block Count Reducer for the lower nine bits of the block count. A second MW module is used for the upper bit only. The following description is relative to the lower order bits.

BLOCK COUNT REGISTER

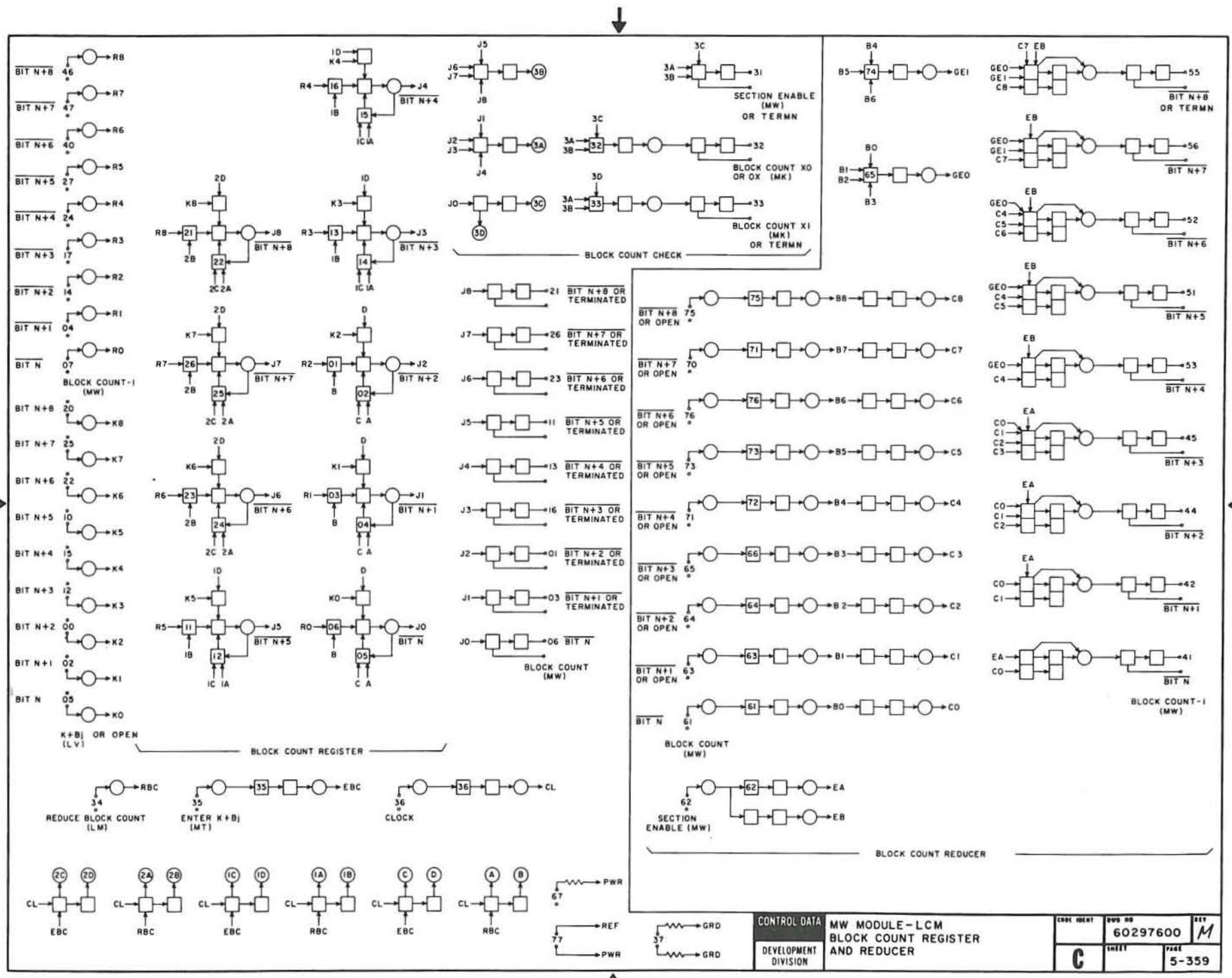
K + Bj Bits 0-8 are complemented and entered in the Block Count Register during a clock period that Enter K + Bj is present. During each following clock period, Block Count-1 Bits 0-8 are entered. This process continues as long as Reduce Block Count is present. The Block Count Register holds the complement of the block count.

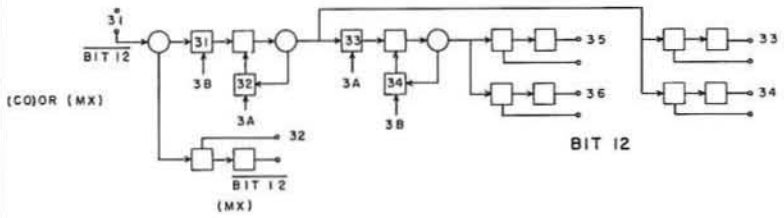
BLOCK COUNT CHECK

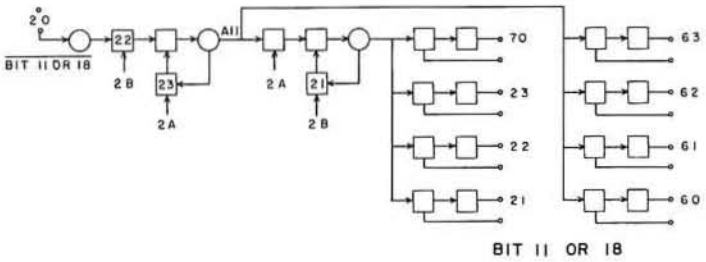
The Block Count Check network translates the contents of the Block Count Register. A Block Count X1 signal is sent to the MK module when the register contains 111111110. A Block Count X0 signal is sent to the MK module when the register contains 111111111. Also, when the register contains all ones a Section Enable signal is sent to the Block Count Reducer of the upper MW module. (Section Enable input for the lower MW module is logical one.)

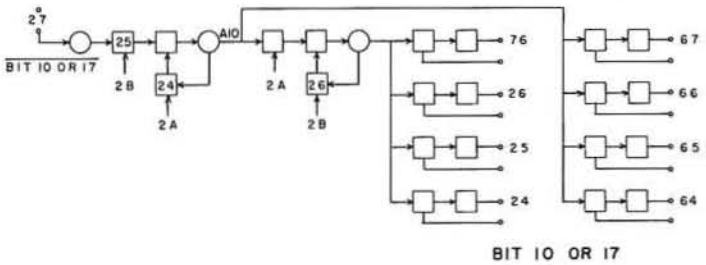
BLOCK COUNT REDUCER

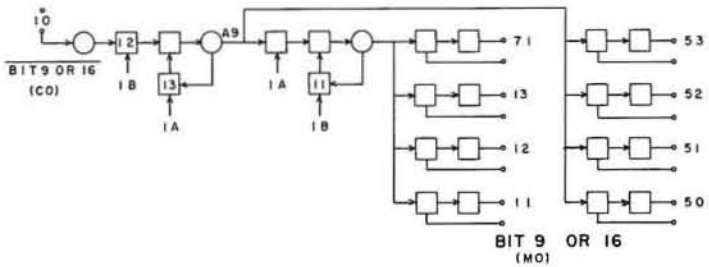
The Block Count Reducer utilizes EXCLUSIVE OR circuits to decrement by one the block count which is held in the Block Count Register. Since this block count is in a complemented form, the Block Count Reducer actually increments by one. For example: if the Block Count Register contains 111111000 (block count equals 7), the Block Count Reducer will output 111111001 (block count equals 6).

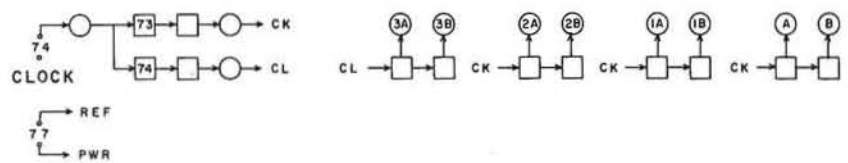

BIT N+8
BIT N+7
BIT N+6
BIT N+5
BIT N+4
BIT N+3
BIT N+2
BIT N+1
BIT N
BLOCK COUNT-1 (MW)
K+Bj OR OPEN (LV)
BLOCK COUNT REGISTER
BLOCK COUNT CHECK
SECTION ENABLE (MW) OR TERMN
BLOCK COUNT XO OR OX (MK)
BLOCK COUNT X1 (MK) OR TERMN
BLOCK COUNT (MW)
BLOCK COUNT REDUCER
REDUCE BLOCK COUNT (LM)
ENTER K+Bj (MT)
CLOCK
SECTION ENABLE (MW)
PWR
REF
GRD
CONTROL DATA
DEVELOPMENT DIVISION
MW MODULE-LCM
BLOCK COUNT REGISTER AND REDUCER
60297600
C
5-359

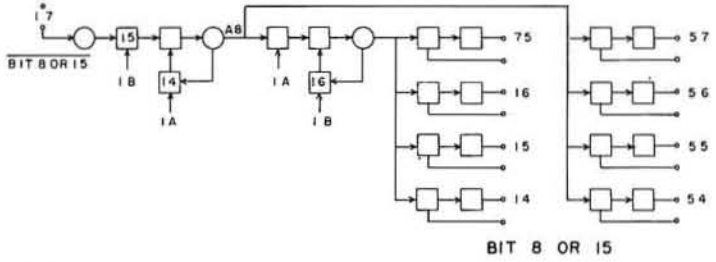


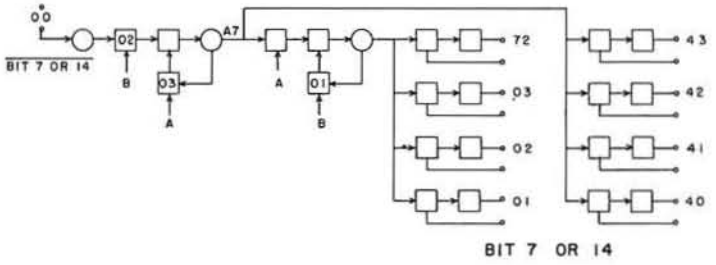


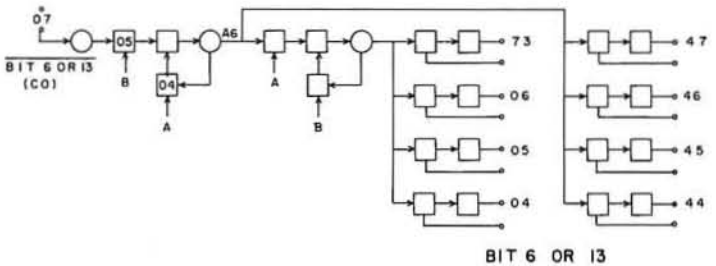






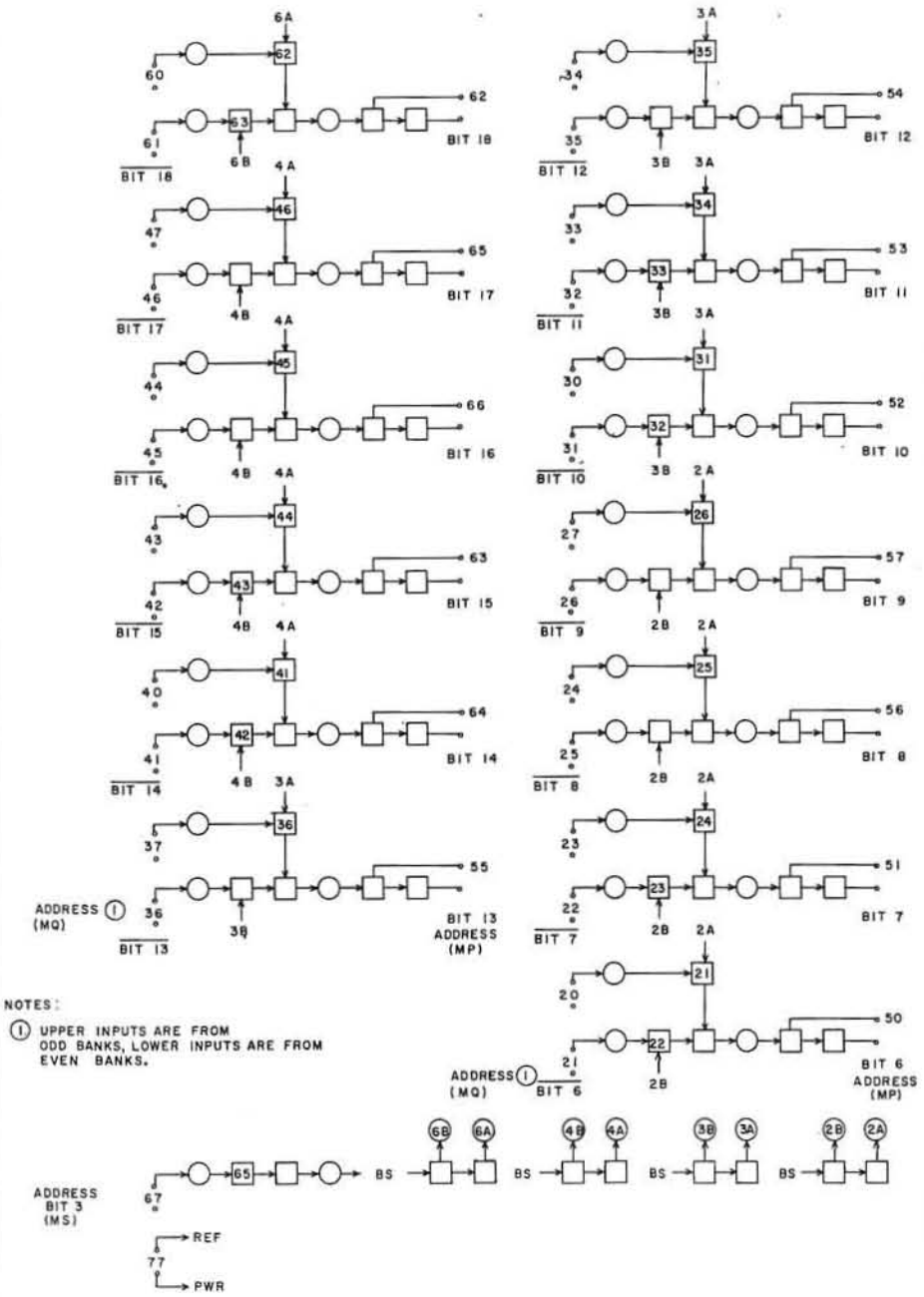






CONTROL DATA	MX MODULE - LCM BANK ADDRESS HOLDING REGISTER AND FANOUT	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	U
			SHEET	PAGE 5-361

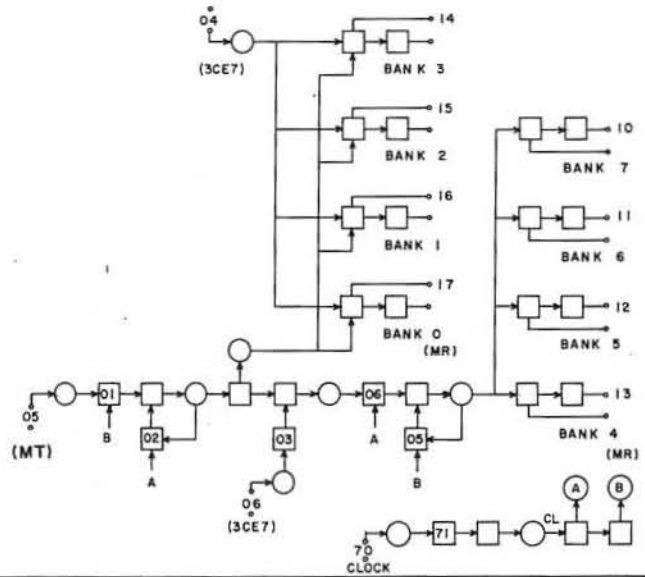
PARITY ADDRESS SELECT



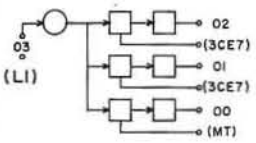
NOTES:

(1) UPPER INPUTS ARE FROM ODD BANKS, LOWER INPUTS ARE FROM EVEN BANKS.

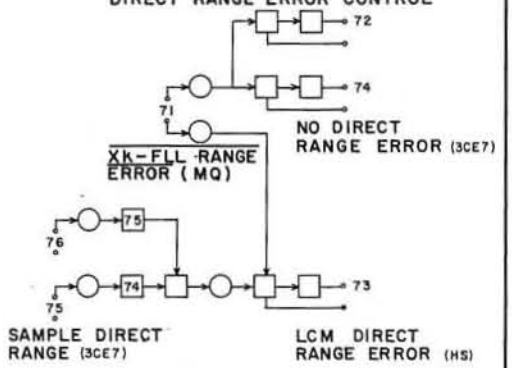
ENTER WRITE FLAGS CONTROL AND FANOUT



MASTER CLEAR FANOUT

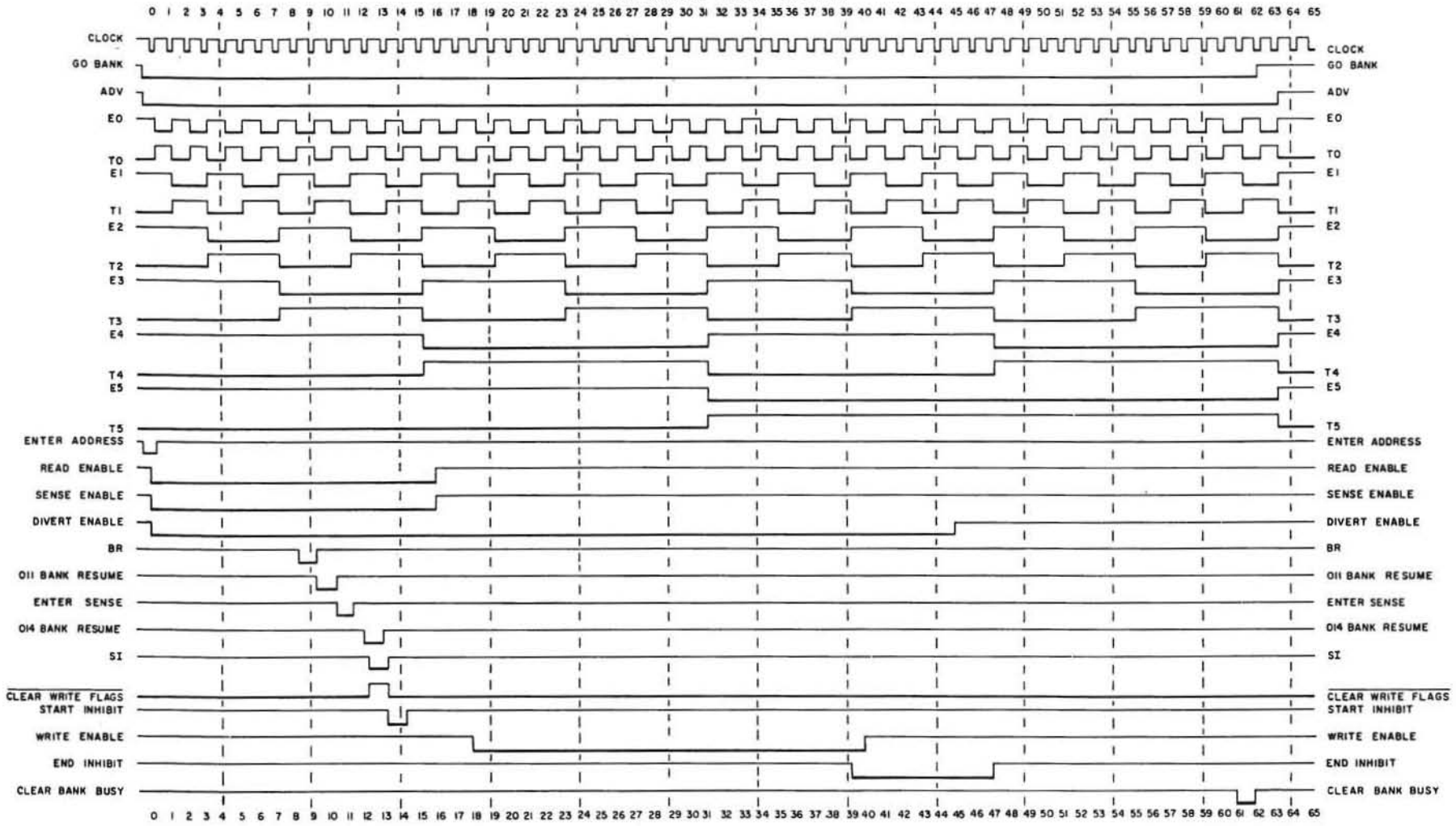


DIRECT RANGE ERROR CONTROL



CONTROL DATA DEVELOPMENT DIVISION	MY MODULE - LCM PARITY ADDRESS SELECTION AND CONTROL FANOUT	CODE IDENT C	DWG NO 60297600	REV AC
			SHEET	PAGE 5-363

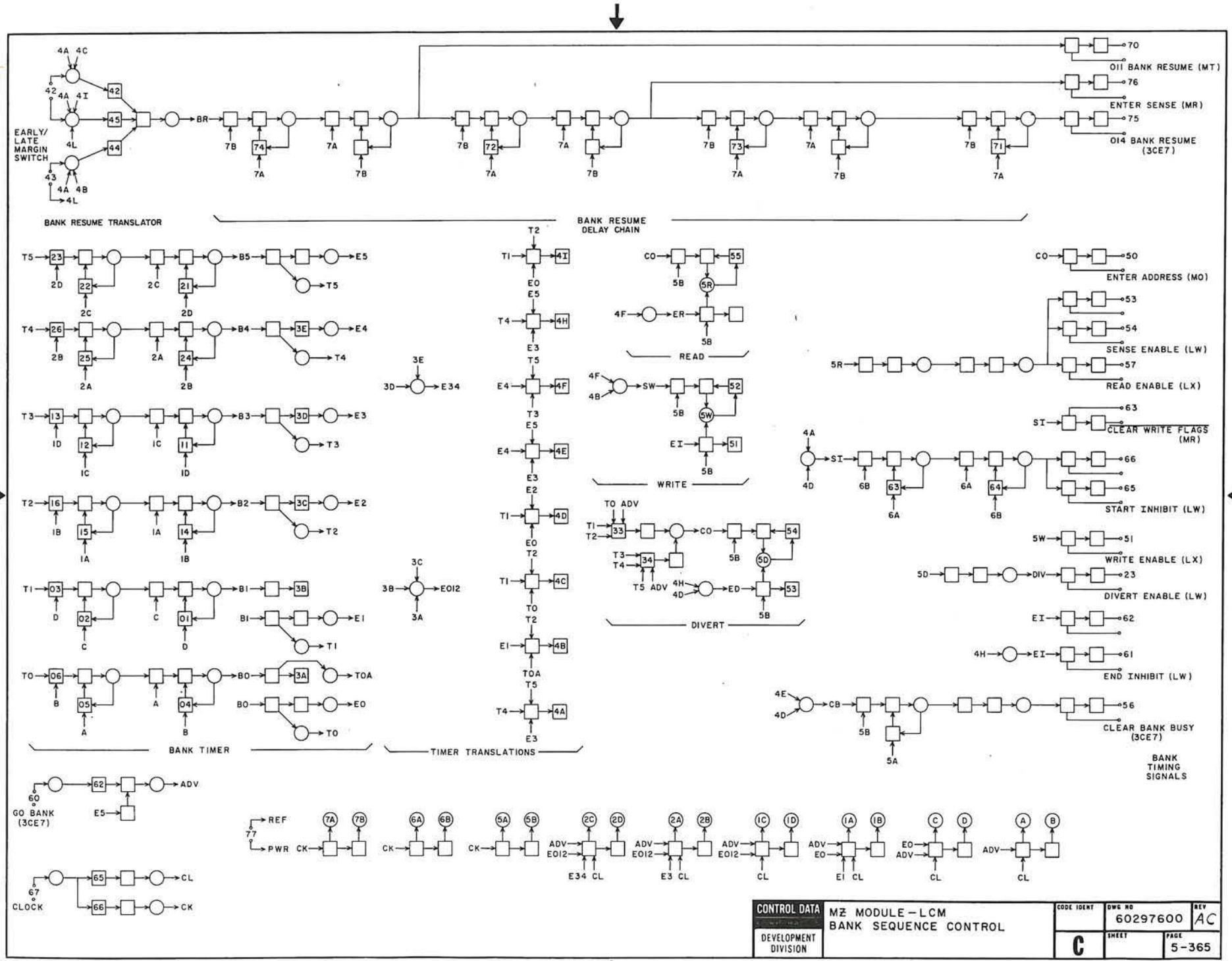
MZ MODULE TIMING DIAGRAM



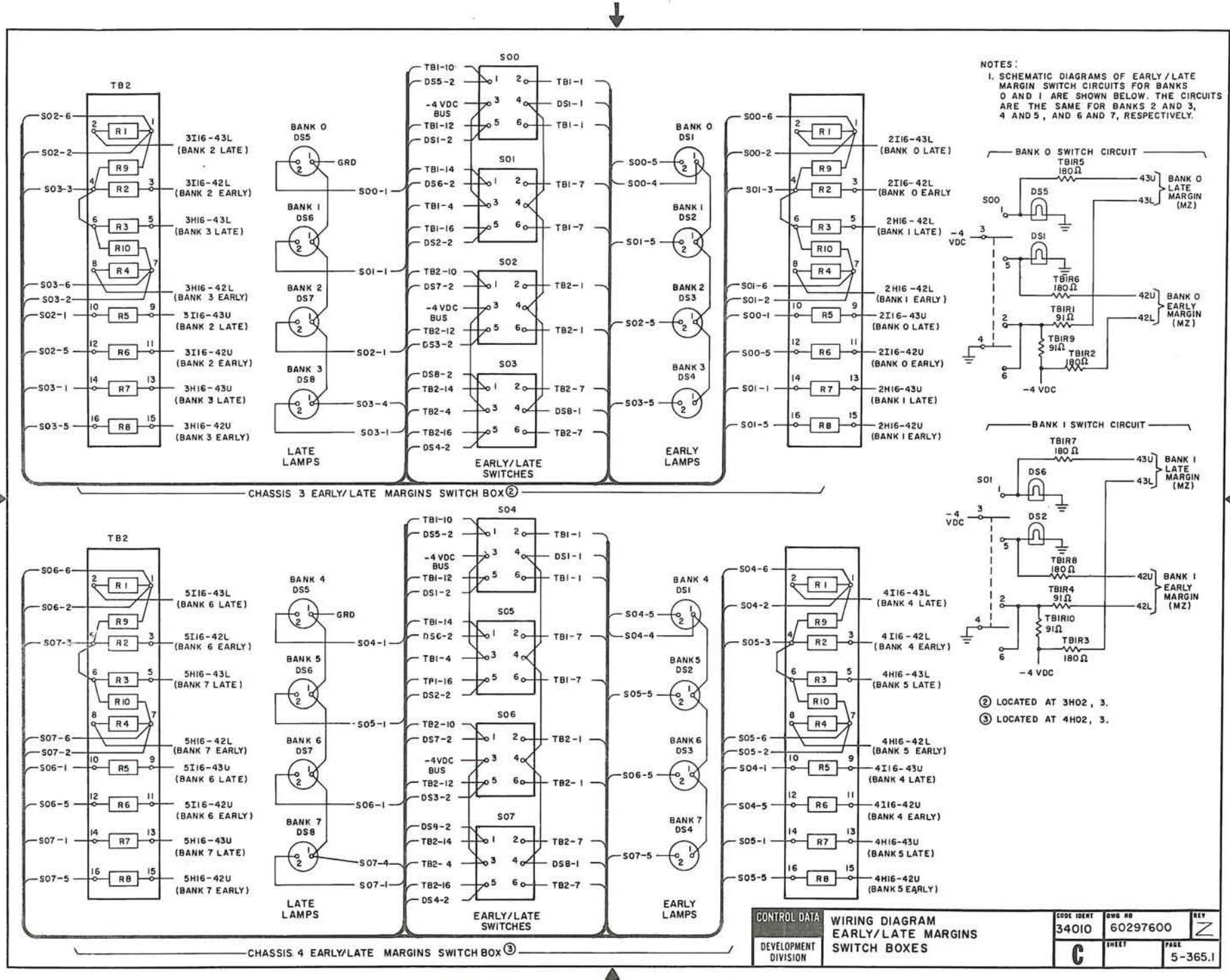
TRANSLATIONS

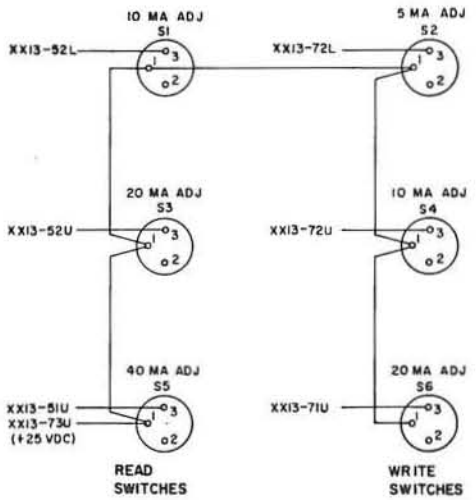
CLOCK: PULSE NUMBERS BEGIN WHEN GO BANK ARRIVES
GO BANK: PRESENT UNTIL CLOCK PULSE AFTER CLEAR BANK BUSY
ADV: GO BANK+E5
E0-E5: OUTPUTS OF BANK TIMER WHICH COUNTS FROM 0-63 DURING BANK READ/WRITE CYCLE
T0-T5: COMPLEMENTED OUTPUTS OF BANK TIMER
ENTER ADDRESS: T5·T4·T3·T2·T1·T0·ADV
READ ENABLE (START): T5·T4·T3·T2·T1·T0·ADV·CLOCK
READ ENABLE (END): T5·E4·T3·CLOCK
SENSE ENABLE (START): T5·T4·T3·T2·T1·T0·ADV·CLOCK
SENSE ENABLE (END): T5·E4·T3·CLOCK
DIVERT ENABLE (START): T5·T4·T3·T2·T1·T0·ADV·CLOCK
DIVERT ENABLE (END): E5·T4·E3·E2·T1·E0
BR (NORMAL-AS SHOWN): T5·T4·E3·T2·T1·E0
BR (EARLY MARGIN-1 CLOCK PERIOD EARLIER THAN SHOWN): T5·T4·E3·T2·T1·T0
BR (LATE MARGIN-1 CLOCK PERIOD LATER THAN SHOWN): T5·T4·E3·T2·E1·T0

011 BANK RESUME: 1 CLOCK PERIOD AFTER BR
ENTER SENSE: 2 CLOCK PERIODS AFTER BR
014 BANK RESUME: 4 CLOCK PERIODS LESS 1 CLOCK PULSE WIDTH AFTER BR
SI: T5·T4·E3·E2·T1·E0
$\overline{\text{CLEAR WRITE FLAGS}}$: SI
START INHIBIT: 1 CLOCK PERIOD AFTER SI
WRITE ENABLE (START): T5·E4·T3·T2·E1·T0·CLOCK
WRITE ENABLE (END): E5·T4·E3·CLOCK
END INHIBIT: E5·T4·E3
CLEAR BANK BUSY (START): E5·E4·E3·E2·T1·E0·CLOCK
CLEAR BANK BUSY (END): CLOCK



CONTROL DATA	MZ MODULE – LCM BANK SEQUENCE CONTROL	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		C	60297600	AC
		SHEET	PAGE	5-365


NOTES:
1. SCHEMATIC DIAGRAMS OF EARLY/LATE MARGIN SWITCH CIRCUITS FOR BANKS 0 AND 1 ARE SHOWN BELOW. THE CIRCUITS ARE THE SAME FOR BANKS 2 AND 3, 4 AND 5, AND 6 AND 7, RESPECTIVELY.
TB2
S02-6
S02-2
S03-3
S03-6
S03-2
S02-1
S02-5
S03-1
S03-5
R1
R9
R2
R3
R10
R4
R5
R6
R7
R8
3I16-43L (BANK 2 LATE)
3I16-42L (BANK 2 EARLY)
3H16-43L (BANK 3 LATE)
3H16-42L (BANK 3 EARLY)
3I16-43U (BANK 2 LATE)
3I16-42U (BANK 2 EARLY)
3H16-43U (BANK 3 LATE)
3H16-42U (BANK 3 EARLY)
BANK 0 DS5
BANK 1 DS6
BANK 2 DS7
BANK 3 DS8
GRD
S00-1
S01-1
S02-1
S03-4
S03-1
LATE LAMPS
S00
S01
S02
S03
TBI-10
DS5-2
-4 VDC BUS
TBI-12
DS1-2
TBI-14
DS6-2
TBI-4
TBI-16
DS2-2
TB2-10
DS7-2
-4 VDC BUS
TB2-12
DS3-2
DS8-2
TB2-14
TB2-4
TB2-16
DS4-2
TBI-1
DS1-1
TBI-1
TBI-7
TBI-7
TB2-1
TB2-1
TB2-7
DS8-1
TB2-7
EARLY/LATE SWITCHES
BANK 0 DS1
BANK 1 DS2
BANK 2 DS3
BANK 3 DS4
S00-5
S00-4
S01-5
S02-5
S03-5
EARLY LAMPS
S00-6
S00-2
S01-3
S01-6
S01-2
S00-1
S00-5
S01-1
S01-5
2I16-43L (BANK 0 LATE)
2I16-42L (BANK 0 EARLY)
2H16-42L (BANK 1 LATE)
2H16-42L (BANK 1 EARLY)
2I16-43U (BANK 0 LATE)
2I16-42U (BANK 0 EARLY)
2H16-43U (BANK 1 LATE)
2H16-42U (BANK 1 EARLY)
CHASSIS 3 EARLY/LATE MARGINS SWITCH BOX ②
BANK 0 SWITCH CIRCUIT
TBIR5 180Ω
TBIR6 180Ω
TBIR1 91Ω
TBIR9 91Ω
TBIR2 180Ω
S00
S01
-4 VDC
43U
43L
42U
42L
BANK 0 LATE MARGIN (MZ)
BANK 0 EARLY MARGIN (MZ)
BANK 1 SWITCH CIRCUIT
TBIR7 180Ω
TBIR8 180Ω
TBIR4 91Ω
TBIR10 91Ω
TBIR3 180Ω
BANK 1 LATE MARGIN (MZ)
BANK 1 EARLY MARGIN (MZ)
② LOCATED AT 3H02, 3.
③ LOCATED AT 4H02, 3.
TB2
S06-6
S06-2
S07-3
S07-6
S07-2
S06-1
S06-5
S07-1
S07-5
5I16-43L (BANK 6 LATE)
5I16-42L (BANK 6 EARLY)
5H16-43L (BANK 7 LATE)
5H16-42L (BANK 7 EARLY)
5I16-43U (BANK 6 LATE)
5I16-42U (BANK 6 EARLY)
5H16-43U (BANK 7 LATE)
5H16-42U (BANK 7 EARLY)
BANK 4 DS5
BANK 5 DS6
BANK 6 DS7
BANK 7 DS8
S04-1
S05-1
S06-1
S07-4
S07-1
LATE LAMPS
S04
S05
S06
S07
EARLY/LATE SWITCHES
BANK 4 DS1
BANK 5 DS2
BANK 6 DS3
BANK 7 DS4
S04-5
S04-4
S05-5
S06-5
S07-5
EARLY LAMPS
S04-6
S04-2
S05-3
S05-6
S05-2
S04-1
S04-5
S05-1
S05-5
4I16-43L (BANK 4 LATE)
4I16-42L (BANK 4 EARLY)
4H16-43L (BANK 5 LATE)
4H16-42L (BANK 5 EARLY)
4I16-43U (BANK 4 LATE)
4I16-42U (BANK 4 EARLY)
4H16-43U (BANK 5 LATE)
4H16-42U (BANK 5 EARLY)
CHASSIS 4 EARLY/LATE MARGINS SWITCH BOX ③
CONTROL DATA
DEVELOPMENT DIVISION
WIRING DIAGRAM
EARLY/LATE MARGINS
SWITCH BOXES
CODE IDENT 34010
DWG NO 60297600
REV Z
SIZE C
SHEET
PAGE 5-365.1

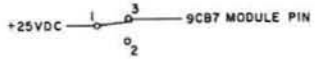


NOTES:

1. THERE IS ONE MEMORY DRIVE CURRENT SWITCH BOX FOR EACH LCM BANK. ONLY ONE IS SHOWN.
2. EXTERNAL CONNECTIONS ARE TO 9CB7 MODULE CONNECTOR ADJACENT TO THE SWITCH BOX.
3. SWITCH BOX AND 9CB7 MODULE LOCATIONS ARE AS FOLLOWS:

BANK	SWITCH BOX	9CB7 MODULE
0	2014	2013
1	2B14	2B13
2	3014	3013
3	3B14	3B13
4	4014	4013
5	4B14	4B13
6	5014	5013
7	5B14	5B13

4. SWITCH SCHEMATIC IS AS FOLLOWS:



CONTROL DATA	WIRING DIAGRAM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	MEMORY DRIVE CURRENT SWITCH BOX	C	60297600	
		SHEET	PAGE 5-365.3	

SECTION 5

PART 6

FLOATING DIVIDE FUNCTIONAL UNIT

PRIMARY BLOCK DIAGRAM
DIVIDE UNIT

The Floating Divide Unit executes the two CPU instructions, 44 and 45, the floating divide and round floating divide respectively. These instructions direct the computer to divide Xj by the divisor Xk and send the quotient to Xi. This unit involves a 17 step iterative process to form the quotient from the two operands. Only one divide instruction may be executed in the iterative portion of the Divide Unit at a given time.

The divide instructions require 20 clock periods for execution. Data moves from the operating registers to the Divide Unit input registers each clock period in which the Divide Busy flag is cleared. This data is used for instruction execution only if a divide instruction issues from the CIW Register and sets the Divide Busy flag. The data which arrives at the Divide Unit during the clock period of instruction issue is then used in the execution of the following divide sequence. The Divide Busy flag prevents the CIW from issuing another divide instruction for the 17 clock periods following instruction issue. However in the 18th clock period after instruction issue a second divide instruction may issue.

Bit 0 of the h designator is held in an input register along with the operand data (Xj) and (Xk). This bit is the Divide Round flag which distinguishes between the two instruction modes.

The Divide Unit operates on positive coefficient values only. Each coefficient for (Xj) and (Xk) is individually complemented in static networks if its sign is negative. The sign of the result is determined by the Divide Unit and is sent to the X Register Input Control unit in the CPU. This sign bit is the logical difference of the two operand sign bits.

The Divide Busy flag initiates a chain of divide sequence control flags which sequence the steps in the instruction execution. This sequence control provides a static condition to distinguish each of the 19 clock periods following the issue of the divide instruction. These static conditions then control the data movement within the divide unit and the data transmission to the X Register input path at the end of the divide sequence.

The format of a floating point number is $k2^n$, where k is a 48-bit integer coefficient and n is a ten-bit integer exponent.

Division of floating point numbers requires the subtraction of the exponents and the division of two 48-bit coefficients. Double precision division is not provided and a remainder cannot be retrieved. Since the divide hardware produces a quotient in the range, 1.7777 7777 7777 7777 through 0.0000 0000 0000 0000, the ratio of Xj to Xk must always be less than 2 to 1. If the divisor is normalized, this requirement is always met. If this requisite is not met, the resulting quotient will be meaningless. If both the dividend Xj and the divisor Xk are normalized, the quotient Xi is also normalized.

The quotient coefficient is formed three bits per clock period in 17 iterative steps. The result of the first iteration is stored in the control module. The results of the 16 succeeding iterations (a total of 48 bits) are stored in the quotient shift register. If the quotient is of the form, 0.X--------X (the ratio of Xj to Xk is less than 1 to 1), the result of the first iteration is a zero and the 48 bits in the quotient shift register are taken as the coefficient of the result:

GIVEN: Xi = Xj/Xk
(Xj) = 2057 4400000000000015
(Xk) = 2032 6000000000000000

The divide coefficient logic forms:

$$\frac{4400000000000015}{6000000000000000} = 0.6000000000000021$$

In floating point format the coefficient must be an integer. Therefore the binary point must be moved 48 places to the right. Since the exponent must be decreased by one for every place the binary point is right shifted, 60_8 is subtracted from the difference of the exponents and the final result is:

(Xi) = 1744 6000000000000021

(NOTE: Final exponent = 2057 - 2032 - 60 = -33 (unbiased) = 1744)

If the quotient is of the form, 1.X--------X (the ratio of Xj to Xk is 1 to 1 or greater, but less than 2 to 1), the result of the first iteration is a one, and the upper 47 bits in the shift register are taken as bits 0-46 of the quotient coefficient. The X Register Access Control takes bit 47 to be a one:

GIVEN: Xi = Xj/Xk

(Xj) = 2016 7000000000000000

(Xk) = 2025 4000000000000000

The Divide logic forms:

$$\frac{7000000000000000}{4000000000000000} = 1.6000000000000000$$

In order to make this quantity an integer, the binary point must be moved 47 places to the right. 57_8 is therefore subtracted from the difference of the exponents and the final result is:

(Xi) = 1711 7000000000000000

(NOTE: Final exponent = 2016 - 2025 - 57 = -66 (unbiased) = 1711)

If the ratio of Xj to Xk is 2 to 1 or greater, the result of the first iteration is forced to a two by the Release Remainder control signal. The control network then sends a special case signal (Indefinite) to the X Register Input Control network along with an operand consisting of all ones. The X Register Input Control network then generates an indefinite result.

COEFFICIENT FORMATION

The quotient coefficient is formed three bits per clock period. The iteration network functions exactly like a pencil and paper octal divide. A multiplication network forms seven multiples of the divisor, Xk through 7Xk. The dividend is entered into the Remainder Register, which holds 51 bits (initially bits 48, 49, and 50 are all 0). The trial subtraction network simultaneously compares each of the seven divisor multiples with the contents of the Remainder register. The largest multiple that is smaller than the remainder is subtracted from the remainder. The resulting quantity is left shifted three binary or one octal position and entered into the Remainder Register. The number of the multiple chosen (Pick Number) becomes the first quotient digit. Pencil and paper method:

```
                                        0.6000 0000 0000 0021
6000 0000 0000 0000 | 4400 0000 0000 0015.0000 0000 0000 0000
                      0000 0000 0000 0000
                    ---------------------
                      4400 0000 0000 0015 0
                      4400 0000 0000 0000 0
                    ---------------------
```

The same division as performed by the functional unit:	15 0000 0000 0000 000
	14 0000 0000 0000 000
Dividend (Xj) = 4400 0000 0000 0015	1 0000 0000 0000 0000
	6000 0000 0000 0000
Divisor (Xk) = 6000 0000 0000 0000	2000 0000 0000 0000

The multiplication network forms:

```
 Xk =  6000 0000 0000 0000
2Xk = 1 4000 0000 0000 0000
3Xk = 2 2000 0000 0000 0000
4Xk = 3 0000 0000 0000 0000
5Xk = 3 6000 0000 0000 0000
6Xk = 4 4000 0000 0000 0000
7Xk = 5 2000 0000 0000 0000
```

The dividend enters the remainder register.

RMDR = 0 4400 0000 0000 0015

Initially, the quotient shift register has contents: XXXX XXXX XXXX XXXX

The 17 iterative operations are performed as follows:

(1) Compare RMDR vs Xk through 7Xk:

RMDR is smaller than any of them.

Enter octal digit "0" in shift register:

Quotient = XXXX XXXX XXXX XXX0 (The quotient is left shifted one octal digit each clock period.) Enter chosen digit (in this example a 0) in control module this iteration only.

Enter RMDR-0 and left shift three:

RMDR = 4 4000 0000 0000 0150 ← becomes a 4 if instruction 45 (only in this iteration)

↑ enter 0 since left shift three

(2) Compare RMDR vs Xk through 7Xk: $6Xk \leq RMDR < 7Xk$

Enter second octal digit: QUOT = XXXX XXXX XXXX XX06

Enter RMDR-6Xk and left shift three: RMDR = 0 0000 0000 0000 150(

(3-14) In the next 12 iterations, an octal digit 0 is picked, and the quotient and remainder are left shifted three binary places each clock period.

RMDR = 0 1500 0000 0000 0000

QUOT = XX06 0000 0000 0000

(15) Compare RMDR vs Xk through 7Xk: RMDR<Xk

Enter octal digit 0: QUOT = X060 0000 0000 0000

Enter RMDR-0: RMDR = 1 5000 0000 0000 0000

(16) Compare RMDR vs Xk through 7Xk: $2Xk \leq RMDR < 3Xk$

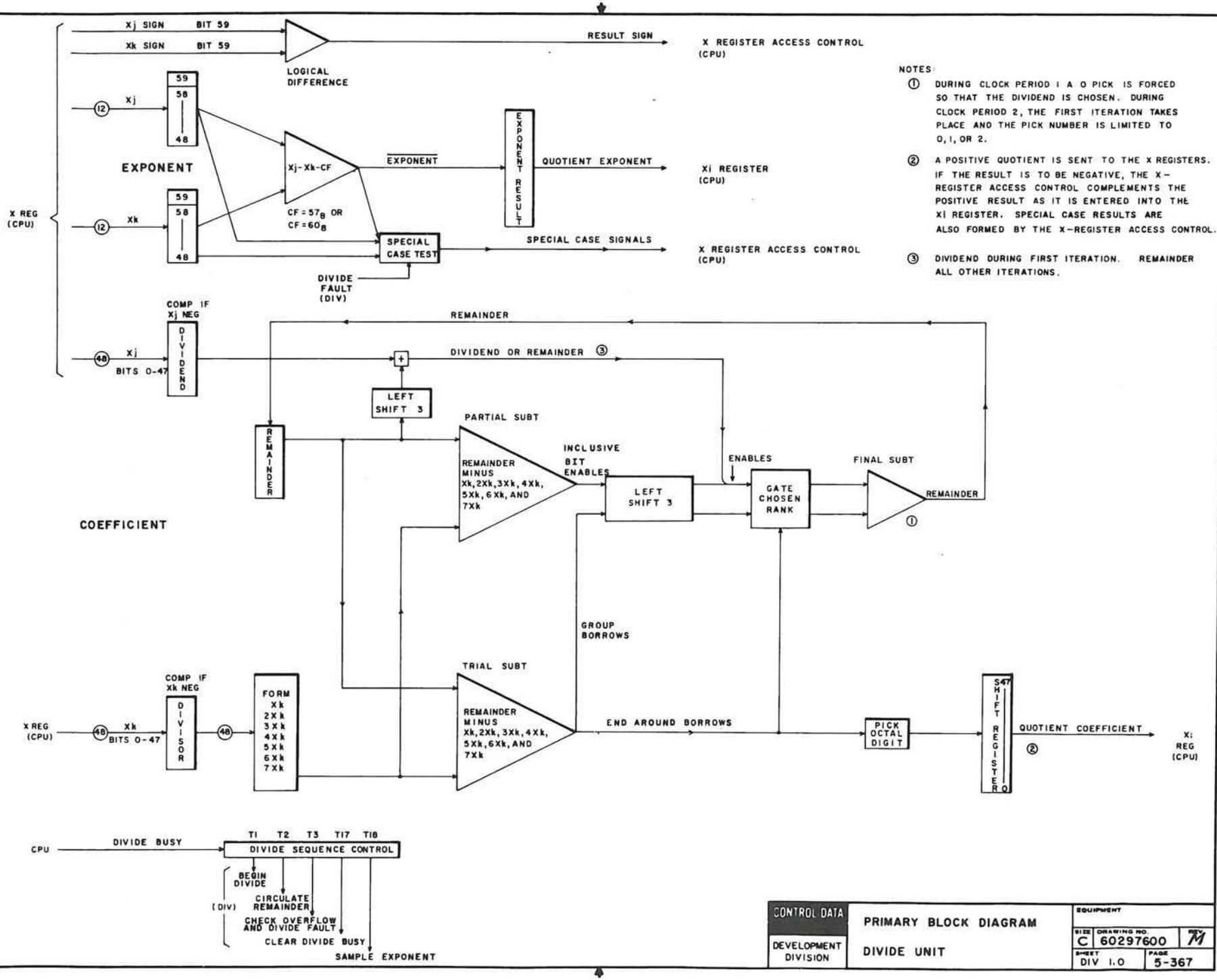
Enter octal digit 2: QUOT = 0600 0000 0000 0002

Enter RMDR-2XK: RMDR = 1 0000 0000 0000 0000

(17) Compare RMDR vs Xk through 7Xk: $Xk \leq RMDR < 2Xk$

Enter octal digit 1: QUOT = 6000 0000 0000 0021

Discard remainder and transmit quotient to Xi Register.



NOTES:

① DURING CLOCK PERIOD 1 A 0 PICK IS FORCED SO THAT THE DIVIDEND IS CHOSEN. DURING CLOCK PERIOD 2, THE FIRST ITERATION TAKES PLACE AND THE PICK NUMBER IS LIMITED TO 0, 1, OR 2.

② A POSITIVE QUOTIENT IS SENT TO THE X REGISTERS. IF THE RESULT IS TO BE NEGATIVE, THE X-REGISTER ACCESS CONTROL COMPLEMENTS THE POSITIVE RESULT AS IT IS ENTERED INTO THE Xi REGISTER. SPECIAL CASE RESULTS ARE ALSO FORMED BY THE X-REGISTER ACCESS CONTROL.

③ DIVIDEND DURING FIRST ITERATION. REMAINDER ALL OTHER ITERATIONS.

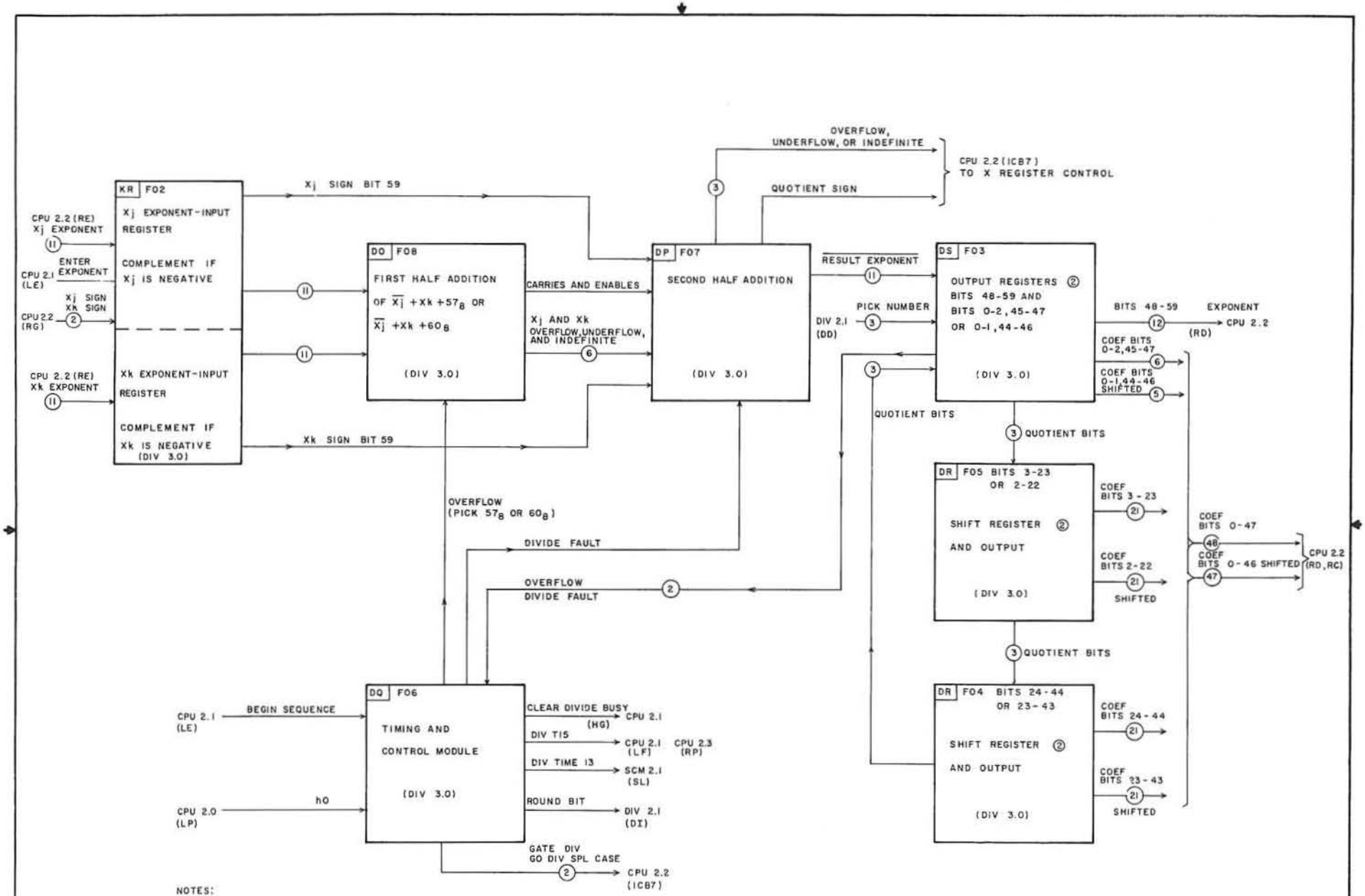
CONTROL DATA DEVELOPMENT DIVISION	PRIMARY BLOCK DIAGRAM DIVIDE UNIT	EQUIPMENT SIZE C · DRAWING NO. 60297600 · REV M SHEET DIV 1.0 · PAGE 5-367

SECONDARY BLOCK DIAGRAM
EXPONENT AND CONTROL NETWORKS

The operand exponents, bits 48-59 of Xj and Xk, are gated into the input registers on the KR module during CP01 and are held there until the end of CP18. The sign bits, bits 59, are sensed and the exponents are individually complemented, if negative.

The subtraction of the exponents is performed by the DO and DP modules. During CP04 the subtraction process uses an overflow correction factor that was determined by the first coefficient iteration in CP02. The exponent is formed and held while the sixteen succeeding coefficient iterations occur. If the first octal digit picked in the DD module is a one, the overflow bit will be a one and 57_8 will be the correction factor. Otherwise the overflow bit will be a zero and 60_8 will be the correction factor. The exponent generated is the result of the divisor exponent and the correction factor being subtracted from the dividend exponent. This is accomplished by complementing the dividend exponent and adding it to the divisor exponent and the correction factor. The sum generated by the DO and DP modules is the complement of the desired result. The output is complemented on the DS module to give the desired result.

The special case determination is shared by the DO and DP modules. The DQ module times the divide sequence and controls the data flow. The output registers for both the exponent and coefficient are on the DS and DR modules. The quotient coefficient is entered into the output registers three bits at a time. Every clock period the coefficient is left shifted three places and three new bits are entered. When the full coefficient is assembled in CP19, both the exponent and the coefficient are gated to the Xi Register.


KR F02
Xj EXPONENT-INPUT REGISTER
COMPLEMENT IF Xj IS NEGATIVE
Xk EXPONENT-INPUT REGISTER
COMPLEMENT IF Xk IS NEGATIVE (DIV 3.0)
CPU 2.2 (RE) Xj EXPONENT
CPU 2.1 (LE) ENTER EXPONENT
CPU 2.2 (RG) Xj SIGN Xk SIGN
CPU 2.2 (RE) Xk EXPONENT
Xj SIGN BIT 59
Xk SIGN BIT 59
DO F08
FIRST HALF ADDITION OF $\overline{Xj}+Xk+57_8$ OR $\overline{Xj}+Xk+60_8$
(DIV 3.0)
CARRIES AND ENABLES
Xj AND Xk OVERFLOW, UNDERFLOW, AND INDEFINITE
DP F07
SECOND HALF ADDITION
(DIV 3.0)
OVERFLOW, UNDERFLOW, OR INDEFINITE
QUOTIENT SIGN
CPU 2.2 (ICB7) TO X REGISTER CONTROL
RESULT EXPONENT
DIV 2.1 (DD) PICK NUMBER
DS F03
OUTPUT REGISTERS (2) BITS 48-59 AND BITS 0-2, 45-47 OR 0-1, 44-46
(DIV 3.0)
BITS 48-59 EXPONENT → CPU 2.2 (RD)
COEF BITS 0-2, 45-47
COEF BITS 0-1, 44-46 SHIFTED
QUOTIENT BITS
DR F05 BITS 3-23 OR 2-22
SHIFT REGISTER (2) AND OUTPUT
(DIV 3.0)
COEF BITS 3-23
COEF BITS 2-22 SHIFTED
DR F04 BITS 24-44 OR 23-43
SHIFT REGISTER (2) AND OUTPUT
(DIV 3.0)
COEF BITS 24-44
COEF BITS 23-43 SHIFTED
COEF BITS 0-47
COEF BITS 0-46 SHIFTED
CPU 2.2 (RD, RC)
OVERFLOW (PICK 57_8 OR 60_8)
DIVIDE FAULT
OVERFLOW DIVIDE FAULT
DQ F06
TIMING AND CONTROL MODULE
(DIV 3.0)
CPU 2.1 (LE) BEGIN SEQUENCE
CPU 2.0 (LP) h0
CLEAR DIVIDE BUSY (HG) → CPU 2.1
DIV TIS → CPU 2.1 (LF) CPU 2.3 (RP)
DIV TIME 13 → SCM 2.1 (SL)
ROUND BIT → DIV 2.1 (DI)
GATE DIV GO DIV SPL CASE → CPU 2.2 (ICB7)

NOTES:

1. ALL MODULES SHOWN ARE LOCATED ON CHASSIS 8.
2. (2) OUTPUT AND SHIFT REGISTERS HOLD THE COMPLEMENT OF THE RESULT.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

SECONDARY BLOCK DIAGRAM
EXPONENT AND CONTROL NETWORKS

EQUIPMENT

SIZE C | DRAWING NO 60297600 | REV AA

SHEET DIV 2.0 | PAGE 5-369

The divide coefficient networks form the quotient of two 48-bit integers. The dividend is Xj; the divisor is Xk; the quotient is Xi. If Xj and Xk are normalized, Xi is normalized. The quotient coefficient is formed three bits (one octal digit) per clock period in the same manner as a pencil and paper octal divide. The quotient may have the form 0.XXXX XXXX XXXX XXXX or 1.XXXX XXXX XXXX XXXX. If the dividend exceeds the divisor by a factor of two or more, a divide fault condition exists and the quotient formed by the coefficient network is ignored. A special case exponent is formed by the X Register Input Control, in this case. A divide fault can occur only if the divisor is not normalized.

For example, in doing a pencil and paper divide the first digit of the quotient is a zero because the dividend is smaller than the divisor.

```
                                        0. 4310 0000 0000 0016
7254 0000 0000 0000  | 4015 3140 0000 0015. 0000 0000 0000 0000
                       3526 0000 0000 0000  0
                     ---------------------  --
                       267 3140 0000 0015  00
                       260 0400 0000 0000  00
                     ---------------------  --
                         7 2540 0000 0015  000
                         7 2540 0000 0000  000
                     ---------------------  ---
                                      15  0000 0000 0000 000
                                       7  2540 0000 0000 000
                                     ---  --------------------
                                       5  5240 0000 0000 0000
                                       5  4010 0000 0000 0000
                                     ---  --------------------
                                          1230 0000 0000 0000
```

The second digit is chosen by comparing multiples of the divisor with the first 17 digits of the remainder. The zero to the right of the dividend is now considered part of the remainder. Since the divisor is now smaller than this new quantity (4015 3140 0000 0015 0), the second digit is not a zero. Since four times the divisor is less than or equal to the remainder and five times the divisor is greater than the remainder, a four is chosen as the next quotient digit. Four times the divisor is now subtracted from the remainder. This difference must be less than the divisor. (If the difference was greater than the divisor, five times the divisor would be less than the remainder.) A zero is added to the right of the difference and the process of comparing this new remainder with the multiples of the divisor and subtracting is repeated. The process is continued until seventeen octal digits are formed for the quotient coefficient.

The following paragraphs describe how the Divide Unit forms the same quotient coefficient.

The networks used in forming the quotient coefficient are:

Input Registers --	Receive divide operand coefficients
Multiplication Networks --	Form multiples of divisor (1Xk - 7Xk)
Trial Subtraction Network --	Subtracts multiples of divisor from dividend (first iteration), or from remainder (all other iterations) to determine which multiples are larger.
Partial Subtraction Network --	Subtracts multiples of divisor from dividend (first iteration), or from current remainder (all other iterations) to begin forming the next remainder.
Final Subtraction network --	Performs final subtraction of the largest multiple that is smaller than the current remainder. The output is a quotient digit (Pick Number) and the new remainder.

INPUT REGISTERS

In the clock period following instruction issue (CP01) the two operands are gated into the coefficient input registers; Xj on the DI modules, Xk on the DJ modules. For the purposes of this explanation, the dividend Xj = 4015 3140 0000 0015. The divisor Xk = 7254 0000 0000 0000.

The dividend (Xj) is complemented and entered into the 51-bit Remainder register on the DA, DB, DC, DD, and DE modules. Bits 48-50 are initially zeros. The divisor (Xk) is sent to the Multiplication network.

MULTIPLICATION NETWORK

The Multiplication network on the DK, DL, DM, and DN modules forms seven multiples of the divisor (Xk). The multiples formed are:

Xk	0	7254	0000	0000	0000
2Xk	1	6530	0000	0000	0000
3Xk	2	6004	0000	0000	0000
4Xk	3	5260	0000	0000	0000
5Xk	4	4534	0000	0000	0000
6Xk	5	4010	0000	0000	0000
7Xk	6	3264	0000	0000	0000

The multiples are used by both the First Stage Trial Subtraction network and the Partial Subtraction network.

TRIAL SUBTRACTION NETWORK

The Trial Subtraction network subtracts each of the seven multiples of the divisor from the dividend (first iteration) or the remainder (all other iterations). If a subtraction produces end around borrow (EAB), that multiple is larger than the remainder (or dividend). The divide unit senses all seven EAB bits to determine which, if any, of the multiples are larger than the remainder.

The first iteration takes place in CP02. For the operands chosen, in this iteration all seven EAB bits are ones, indicating that all seven multiples are larger than the remainder. In this case a zero is the Pick Number generated on the DD module and entered into the shift register (DS module) as the first quotient digit. The remainder is left shifted one octal digit (three bit positions) and re-entered into the Remainder register. Bits 0 - 2 are now zeros. This shifting and entering zeros into the three lowest bits corresponds to adding a zero on the right of the dividend in the pencil and paper divide.

In CP03 the second iteration takes place. Once again each of the seven multiples is subtracted from the remainder by the Trial Subtraction network. The seven EAB bits are sensed by the Final Subtraction network. In this iteration the EAB bits for ranks 1 - 4 are zeros and the EAB bits for ranks 5 - 7 are ones. (Rank refers to the multiple involved. Thus a Rank 4 EAB bit refers to an EAB bit generated by subtracting 4Xk from the remainder). The DD module generates a 4 as the Pick Number because rank 4 is the highest rank with a zero EAB bit.

The Trial Subtraction network has two stages: the first stage is on the DA, DB, DC, DD, and DE modules; the second stage is on the DF and DG modules.

FIRST STAGE TRIAL SUBTRACTION NETWORK

The First Stage Trial Subtraction network receives the remainder, which is held on the same modules, and the seven multiples of the divisor (Xk through 7Xk) from the multiplication networks on the DK, DL, DM, and DN modules. The multiples are subtracted from the remainder to generate group borrows out and group enables. The group borrows out and the group enables are transmitted to the Second Stage Trial subtraction network (DF and DG modules). Since borrows cannot be propagated through bits 0 - 2, the DC module does not generate any group 0 enables. The group 0 borrows generated by the DC modules are transmitted to both the Final Subtraction network and the Second Stage Trial Subtraction network.

SECOND STAGE TRIAL SUBTRACTION NETWORK

One DF module and one DG module handle each rank of the Second Stage Trial Subtraction. Each module in the Second Stage network generates an EAB bit for its rank. However, for a particular rank, the EAB generated by the DF module is the duplicate of the EAB generated by the associated DG module. The DF modules transmit their EAB bits to the Final Subtraction network on the DA and DD modules. The DG modules transmit their EAB bits to the Final Subtraction network on the DB and DE modules.

Each module also generates a group borrow input for seven groups. The DF modules generate borrows for seven different groups than the DG modules. These group borrow inputs are transmitted to the Final Subtraction network on the DA, DB, DD and DE modules where they will be used with inclusive bit enables from the Partial Subtraction network to form the Pick Number and the new remainder.

PARTIAL SUBTRACTION NETWORK

In the pencil and paper divide 4Xk was subtracted from the remainder. In the divide unit the remainder is complemented and added to 4Xk. The resulting sum is complemented to produce the desired difference. In effect, the divide unit forms - (-RMDR + 4Xk) instead of (RMDR - 4Xk). The inclusive bit enables for the intermediate sum are formed by the Partial Subtraction network on the DH modules. The complemented remainder is received from the DC and DA modules. The seven multiples of the divisor from Xk to 7Xk are received from the multiplication network on the DK, DL, DM, and DN modules.

Each DH module adds one digit of the complemented remainder to the corresponding digit of each of the seven multiples. Possible carries between digits are ignored by the Partial Subtraction network, but possible carries between bits are processed. The resulting sums are the inclusive bit enables for ranks 1 - 7. The inclusive bit enables for rank 0 are the true remainder bits. All the inclusive bit enables are left shifted one digit on output from the DH modules.

The inclusive bit enables for ranks 1 - 7 go directly to the Final Subtraction network on the DA, DB, DD, and DE modules. The rank 0 inclusive bit enables (true remainder) are transmitted to the DI and DQ modules. The DI and DQ modules choose either the dividend or the true remainder as the rank 0 inclusive bit enables. In CP01 the dividend is chosen; in CP02 - CP17 the remainder is chosen. Whichever quantity is chosen, the 51 inclusive bit enables are complemented as they are transmitted to the Final Subtraction network on the DA, DB, DC, DD and DE modules.

FINAL SUBTRACTION NETWORK

The Final Subtraction networks adds the group borrow inputs from the Trial Subtraction network to the ranks 1 - 7 inclusive bit enables from the Partial Subtraction network and the rank 0 inclusive bit enables. Thus:

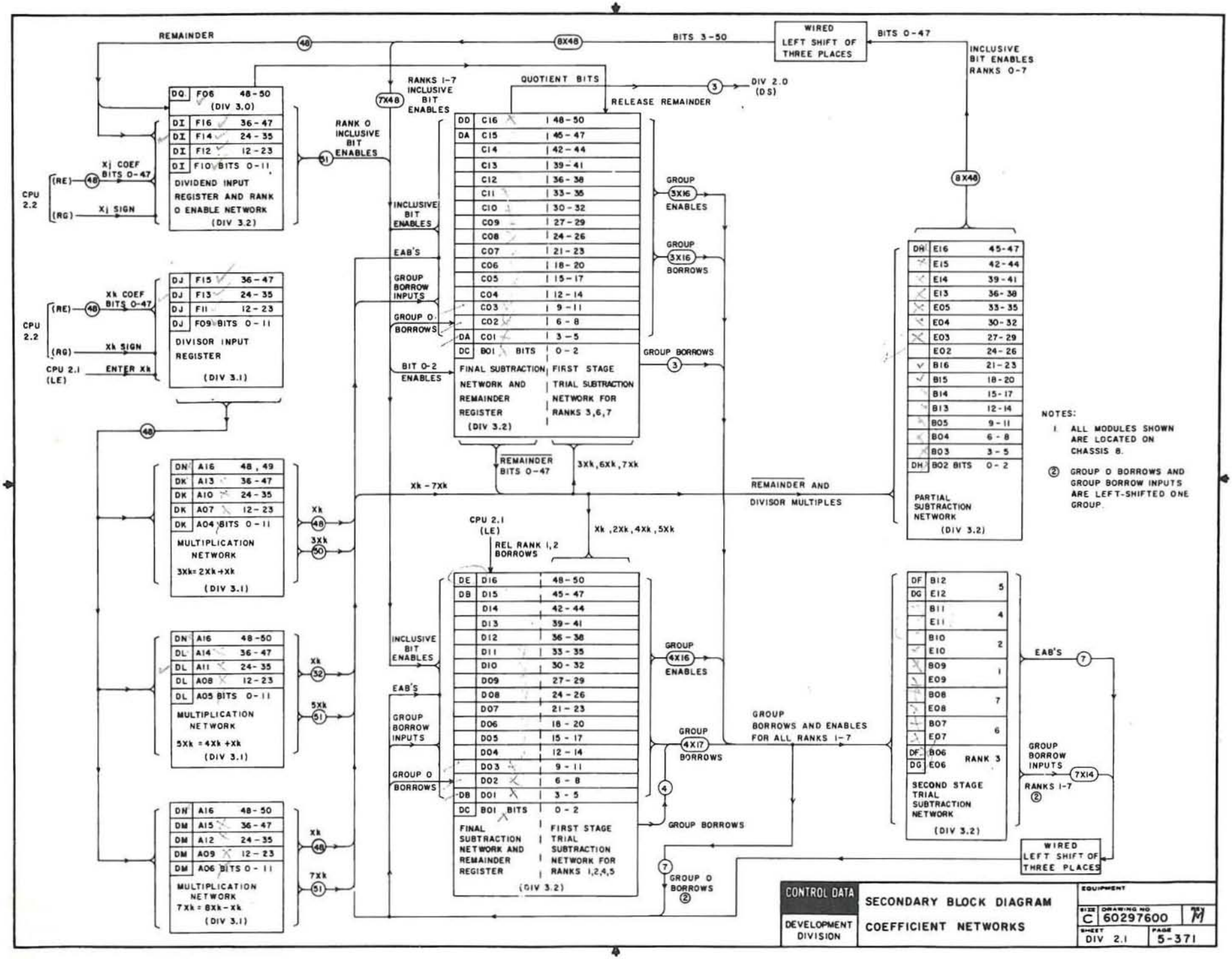
	$\overline{\text{RMDR}}$	
	+4Xk	RMDR
		-4Xk
Inclusive Bit Enables	Results of Partial Subtraction network	DIFF
+ Group Borrows	Results of Trial Subtraction network	
	$\overline{\text{DIFF}}$ Results of Final Subtraction network	
	DIFF Complemented to become DIFF	
	Divide Unit	Pencil and Paper

In the pencil and paper divide a zero is added on the right of the DIFF before the next iteration takes place (before the next digit is picked). In the divide unit the DIFF is left shifted one digit and entered into the Remainder register and bits 0 - 2 become zeros. (The right-most digit becomes a zero).

In the divide unit the DIFF is left-shifted before it is entered into the Remainder register. The left shifting is accomplished by left shifting the inclusive bit enables and the group borrow inputs before the final subtraction. The inclusive bit enables for bits 0 - 2 are forced to ones. Thus, when the Difference is complemented these bits become zeros.

The Final Subtraction network translates the seven EAB bits to determine which multiple was chosen this iteration and gates the Difference for that multiple only to the Remainder register. A translation network on the DD module translates the EAB bits to extract the Pick Number for this iteration and sends it to the coefficient shift register on the DS module.

This process continues until CP18, when the seventeenth iteration takes place. In CP19 the iteration network goes through the motions of forming another quotient, but the output is ignored.


REMAINDER
48
8X48
BITS 3-50
WIRED LEFT SHIFT OF THREE PLACES
BITS 0-47
INCLUSIVE BIT ENABLES RANKS 0-7
RANKS 1-7 INCLUSIVE BIT ENABLES
7X48
QUOTIENT BITS
3
DIV 2.0 (DS)
RELEASE REMAINDER
DQ F06 48-50 (DIV 3.0)
DI F16 36-47
DI F14 24-35
DI F12 12-23
DI F10 BITS 0-11
DIVIDEND INPUT REGISTER AND RANK 0 ENABLE NETWORK (DIV 3.2)
CPU 2.2
(RE) Xj COEF BITS 0-47
(RG) Xj SIGN
RANK 0 INCLUSIVE BIT ENABLES
51
DD C16 48-50
DA C15 45-47
C14 42-44
C13 39-41
C12 36-38
C11 33-35
C10 30-32
C09 27-29
C08 24-26
C07 21-23
C06 18-20
C05 15-17
C04 12-14
C03 9-11
C02 6-8
DA C01 3-5
DC B01 BITS 0-2
FINAL SUBTRACTION NETWORK AND REMAINDER REGISTER (DIV 3.2)
FIRST STAGE TRIAL SUBTRACTION NETWORK FOR RANKS 3,6,7
INCLUSIVE BIT ENABLES
EAB'S
GROUP BORROW INPUTS
GROUP 0 BORROWS
BIT 0-2 ENABLES
GROUP 3X16 ENABLES
GROUP 3X16 BORROWS
GROUP BORROWS
3
8X48
DH E16 45-47
E15 42-44
E14 39-41
E13 36-38
E05 33-35
E04 30-32
E03 27-29
E02 24-26
B16 21-23
B15 18-20
B14 15-17
B13 12-14
B05 9-11
B04 6-8
B03 3-5
DH B02 BITS 0-2
PARTIAL SUBTRACTION NETWORK (DIV 3.2)
NOTES:
1. ALL MODULES SHOWN ARE LOCATED ON CHASSIS 8.
2. GROUP 0 BORROWS AND GROUP BORROW INPUTS ARE LEFT-SHIFTED ONE GROUP.
CPU 2.2
(RE) Xk COEF BITS 0-47
(RG) Xk SIGN
CPU 2.1 (LE) ENTER Xk
DJ F15 36-47
DJ F13 24-35
DJ F11 12-23
DJ F09 BITS 0-11
DIVISOR INPUT REGISTER (DIV 3.1)
48
REMAINDER BITS 0-47
3Xk,6Xk,7Xk
Xk-7Xk
REMAINDER AND DIVISOR MULTIPLES
DN A16 48,49
DK A13 36-47
DK A10 24-35
DK A07 12-23
DK A04 BITS 0-11
MULTIPLICATION NETWORK
3Xk=2Xk+Xk
(DIV 3.1)
Xk
48
3Xk
50
CPU 2.1 (LE)
REL RANK 1,2 BORROWS
Xk,2Xk,4Xk,5Xk
DE D16 48-50
DB D15 45-47
D14 42-44
D13 39-41
D12 36-38
D11 33-35
D10 30-32
D09 27-29
D08 24-26
D07 21-23
D06 18-20
D05 15-17
D04 12-14
D03 9-11
D02 6-8
DB D01 3-5
DC B01 BITS 0-2
FINAL SUBTRACTION NETWORK AND REMAINDER REGISTER
FIRST STAGE TRIAL SUBTRACTION NETWORK FOR RANKS 1,2,4,5
(DIV 3.2)
INCLUSIVE BIT ENABLES
EAB'S
GROUP BORROW INPUTS
GROUP 0 BORROWS
GROUP 4X16 ENABLES
GROUP 4X17 BORROWS
GROUP BORROWS
4
7
GROUP 0 BORROWS 2
DN A16 48-50
DL A14 36-47
DL A11 24-35
DL A08 12-23
DL A05 BITS 0-11
MULTIPLICATION NETWORK
5Xk=4Xk+Xk
(DIV 3.1)
Xk
32
5Xk
51
DN A16 48-50
DM A15 36-47
DM A12 24-35
DM A09 12-23
DM A06 BITS 0-11
MULTIPLICATION NETWORK
7Xk=8Xk-Xk
(DIV 3.1)
Xk
48
7Xk
51
GROUP BORROWS AND ENABLES FOR ALL RANKS 1-7
DF B12 5
DG E12
B11 4
E11
B10 2
E10
B09 1
E09
B08 7
E08
B07 6
E07
DF B06 RANK 3
DG E06
SECOND STAGE TRIAL SUBTRACTION NETWORK (DIV 3.2)
EAB'S
7
GROUP BORROW INPUTS
7X14
RANKS 1-7
2
WIRED LEFT SHIFT OF THREE PLACES
CONTROL DATA
DEVELOPMENT DIVISION
SECONDARY BLOCK DIAGRAM
COEFFICIENT NETWORKS
EQUIPMENT
SIZE C
DRAWING NO. 60297600
REV M
SHEET DIV 2.1
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EXPONENT MANIPULATION

INPUT REGISTERS

The data input registers for both operand exponents, bits 48-59, are on the KR module. These registers are of the clear enter type. They are cleared and new data is entered every clock period in which the control signal is a one. The data that is in the registers when the Divide Busy flag sets is held statically for the seventeen clock periods during which the flag remains set. Bit 59 of Xj and bit 59 of Xk are sensed and the exponents (bits 48-58) are individually complemented if they are negative. The KR output goes to the DO module (bits 48-58) and the DP module (bit 59).

EXPONENT FORMATION

The exponent subtraction occurs while the coefficient is being formed. The quotient exponent is held statically until the quotient coefficient is completely assembled. The exponent subtraction network, comprised of the Preliminary and Final addition networks, is on the DO and DP modules. Instead of subtracting the divisor exponent and the correction factor from the dividend exponent, the dividend exponent is complemented and added to the divisor exponent and to the correction factor (CF). The correction factor is determined in CP04 by bit 0 (overflow bit) of the first quotient coefficient digit. The resulting sum ($\overline{\text{Exponent}}$) is complemented on output by the DS module to obtain the quotient exponent. In effect the exponent network forms - (-Xj + Xk + CF) instead of (Xj - Xk - CF).

The exponent addition is performed in two halves. The network that performs the preliminary exponent addition is on the DO module; the final exponent addition network is on the DP module. The bias is removed from both exponents on input to the DO module. The exponents and the correction factor are then added. If the Overflow bit from the DQ module, bit 0 of the first iteration, is a zero, the quotient is of the form 0. XXXX XXXX XXXX XXXX and the correction factor is 60_8. If bit 0 of the first iteration is a one, the quotient is of the form 1. XXXX XXXX XXXX XXXX, and the correction factor is 57_8. The result of the first half addition is a bit carry and a bit enable for each position. These bits are transferred to the final exponent addition network on the DP module.

The Final addition network combines the carries and enables in a 13-bit mode. The two extra bits are formed by sign-extending the exponents. The upper three bits of the 13-bit sum are sensed to detect special case conditions. Exponent bias is added, then the lower eleven bits of the sum are transferred to the output network on the DS module.

The sign of the quotient is formed by a network on the DP module and is sent to the X Register Input Control. This sign bit is the logical difference of the two operand sign bits. A network on the DO module checks for operand exponent overflow, underflow, and indefinite exponents. The rest of the special case checks are performed on the DP module. If any special case exists the special case signal to the DQ module will be a one, in which case a quotient of all ones will be sent to the X Register. The three signals to the X Register Input Control specify which, if any, of the special case conditions exist.

SPECIAL CASE

A number of special cases are treated in the Floating Divide Unit. If any special case conditions exist the Special Case signal from DP to the DQ module becomes a one. The Go Divide Special Case signal from DQ to the X Register Input Control becomes a one and the specific condition is indicated by the exponent Indefinite, Overflow, and Underflow signal from the DP module. In any special case condition the transmission of data from the Divide Unit output registers to the destination X Register is blocked. The Gate Quotient signal from DQ to DS remains a zero, forcing the exponent output registers to transmit all ones. The Gate Output signal (which is the Gate Quotient signal delayed one clock period) forces the coefficient output registers to transmit all ones. Thus a quotient of all ones is delivered to the X Register and the input control forms the particular special case word (see Appendix B, Pub No. 60258200 for a table of special case operands). The special condition flags cause the appropriate error condition flag to be set in the PSD Register.

If no special case conditions exist the Special Case signal from DP to DQ remains a zero. The Go Divide Special Case signal to the X Register Input Control is a zero and the Gate Divide and the Gate Quotient signals are ones. The Gate Quotient signal gates the quotient output.

SPECIAL CASE OPERANDS

One category of special case conditions involves overflow, underflow, or indefinite operand values. These situations are sensed in the DO module. The combinations of special operand values which cause specific results are sensed on the DP module. If either operand is indefinite, or if both operands are indefinite, the result is indefinite. The operand coefficients are ignored in this case, and the resulting word delivered to the Xi Register is positive indefinite with a zero coefficient. The Indefinite Condition flag is set in the PSD register for this case.

If Xj has an overflow exponent and Xk is in floating point range or has an underflow exponent, the result is a complete overflow word delivered to the Xi Register. The coefficients of the operands are ignored in this case, and the result is a zero coefficient. The sign of the result is calculated in the same manner as for operands in range. The Overflow Condition flag is set in the PSD register for this case.

If Xj has an underflow exponent and Xk is in floating point range or has an overflow exponent, the result is a complete underflow word delivered to the Xi Register. The coefficients of the operands are ignored in this case, and the result is a zero word. The sign of the result is calculated in the same manner as for operands in range. The Underflow Condition flag is set in the PSD register for this case.

If Xk has an overflow exponent and Xj is in floating point range the result is a complete underflow word delivered to the Xi Register. The coefficients of the operands are ignored in this case, and the result is a zero word. The sign of the result is calculated in the same manner as for operands in range. The Underflow Condition flag is set in the PSD register for this case.

If Xk has an underflow exponent and Xj is in floating point range the result is a complete overflow word delivered to the Xi register. The coefficients of the operands are ignored in this case, and the result has a zero coefficient. The sign of the result is calculated in the same manner as for operands in range. The Overflow Condition flag is set in the PSD Register for this case.

The combination of operand exponents of overflow divided by overflow and underflow divided by underflow result in a positive indefinite word with a zero coefficient delivered to the Xi Register. The Indefinite Condition flag is set in the PSD Register for this case.

SPECIAL CASE QUOTIENT

A second category of special cases occur if there is an underflow, or an overflow, of the floating point exponent range during the exponent calculation in the Divide Unit. In these cases the special case result is indicated to the X Register Input Control unit, and the output from the Divide Unit is blocked in the same manner as for the special case operands.

A complete overflow occurs for this instruction whenever the exponent computation results in an exponent greater that +1777 octal (unbiased). If any combination of operand exponents causes an indefinite condition, the overflow situation is ignored. Otherwise this situation is sensed as a special case and a complete overflow word with proper sign, overflow exponent, and zero coefficient is delivered to the Xi Register. The coefficient calculation is ignored for this case, and the Overflow Condition flag is set in the PSD Register.

A complete underflow occurs for this instruction whenever the exponent computation results in an exponent less than -1777 octal (unbiased). If any combination of operand exponents causes an indefinite condition, this underflow situation is ignored. Otherwise this situtation is sensed as a special case, and a complete zero word with proper sign is delivered to the Xi Register. The coefficient calculation is ignored in this case, and the Underflow Condition flag is set in the PSD Register.

SPECIAL CASE -- DIVIDE FAULT

A third special case category occurs if the dividend coefficient is larger than the divisor by a factor of two or more. This is a divide fault situation which can occur if the divisor is not normalized. The initial trial subtraction in the coefficient calculation results in an octal digit with a value of two. If an overflow or underflow condition does not exist, an indefinite condition result is indicated for this case, and it is treated in the same manner as the other special cases.

If an overflow or an underflow condition does exist, the divide fault situation is ignored.

PARTIAL OVERFLOW OR UNDERFLOW

A partial overflow occurs for this instruction whenever the exponent computation results in exactly +1777 octal (unbiased). There are no error condition flags set in the PSD Register for this case, and the result is delivered to the Xi Register in a normal manner. Subsequent use of this result as an operand in a floating point unit may, however, result in overflow detection.

A partial underflow occurs for this instruction whenever the exponent computation results in exactly -1777 octal (unbiased). There are no error condition flags set in the PSD Register for this case, and the result is delivered to the Xi Register in a normal manner. Subsequent use of this result as an operand in a floating point unit may, however, result in underflow detection.

OUTPUT

The Exponent Output register is on the DS module. The complemented 11-bit biased quotient exponent is delivered from the DP final addition network. In CP18 a Gate Quotient signal from the DQ module enables a clock gate so that the exponent will enter the output register. The exponent is complemented on output because the exponent network forms the complement of the quotient exponent.

Since a positive quotient is delivered to the X Register, bit 59 is entered as a zero. The absence of a Gate Quotient signal in CP18 indicates that one of the special case conditions exists, in which case, an exponent of 12 ones is delivered to the X register.

The quotient coefficient is assembled three bits per clock period in the 48-bit shift register. In each of CP03-CP19 an octal digit is delivered from DD to DS. After 17 iterations, the DS module has bits 0-2 and 45-47; the two DR modules have bits 3-44. Every clock period the quotient is left shifted three places, three new quotient bits from DD enter from the iteration network, and the upper three bits are discarded. After 17 iterations the shift register contains 48 bits of data. Bits 0 and 1 of the octal digit formed in the first iteration are stored in the DQ module. If bit 1 is a one, a Divide Fault condition (The dividend exceeds the divisor by a factor of two or more) exists. If this condition or any other special case condition exists, the Gate Quotient signal will remain a zero and the delivery of the quotient will be blocked. As a result a coefficient of all ones will be on the lines to the X Register in CP19. If bit 1 is a zero and no other special case conditions exist, the Gate Quotient signal will become a one in CP18 and the quotient coefficient will be delivered to the X Register during CP19.

If bit 0 of the first iteration digit is a zero, the quotient is of the form 0. XXXX XXXX XXXX XXXX. In this case a correction factor of 48 is subtracted from the exponent, the overflow bit is a zero, and the 48 bits in the shift register are delivered to the X Register.

If bit 0 of the first iteration digit is a one, the quotient is of the form 1. XXXX XXXX XXXX XXXX. In this case a correction factor of 47 is subtracted from the exponent. The Overflow bit becomes a one, causing a one-bit right shift of the coefficient output. The upper 47 bits in the shift register are delivered to the X Register as bits 0-46. In this case the bit 47 output is blocked. Therefore bit 47 is entered as a one. All outputs are timed to occur in CP19.

CONTROL

The divide sequence control on the DQ module times the entire divide instruction. The clock periods on the left of the Divide Sequence Control box indicate the times that a significant signal arrives at the module. The times on the right are the clock periods of departure of significant signals.

The three Remainder bits are part of the coefficient iteration network. They are used as rank 0 bit enables in the DD and DE modules.

The Special Case signal indicates a special case exponent. The Gate Divide and Go Divide signals go to the X Register Input Control to gate in the appropriate data. The Gate Quotient signal causes the quotient to be delivered in CP19.

The Begin Sequence signal initiates the divide timing sequence. The Divide Fault signal is bit 1 of the first coefficient iteration digit. This bit is sent to the DP module where it forces a Special Case condition if it is a one.

The Overflow bit is bit 0 of the first coefficient iteration digit. This bit goes to the DO module where it determines the correction factor. It also goes to the DR and DS modules where it determines which 48 bits of the coefficient are delivered to the X Register.

The Divide Round flag (h0) is set in the Floating Divide Unit at the end of a clock period in which a Round Floating Divide instruction issues from the CIW register. This flag modifies the dividend in the third clock period of instruction execution. An octal digit with a value of four is entered in the lowest order bits of the remainder register if this flag is set. This occurs only for the one clock period. Zero bits are entered in these bit positions during all other clock periods in the divide sequence. This modification of the dividend has the effect of increasing the dividend value by one half of the least significant bit in the original operand.

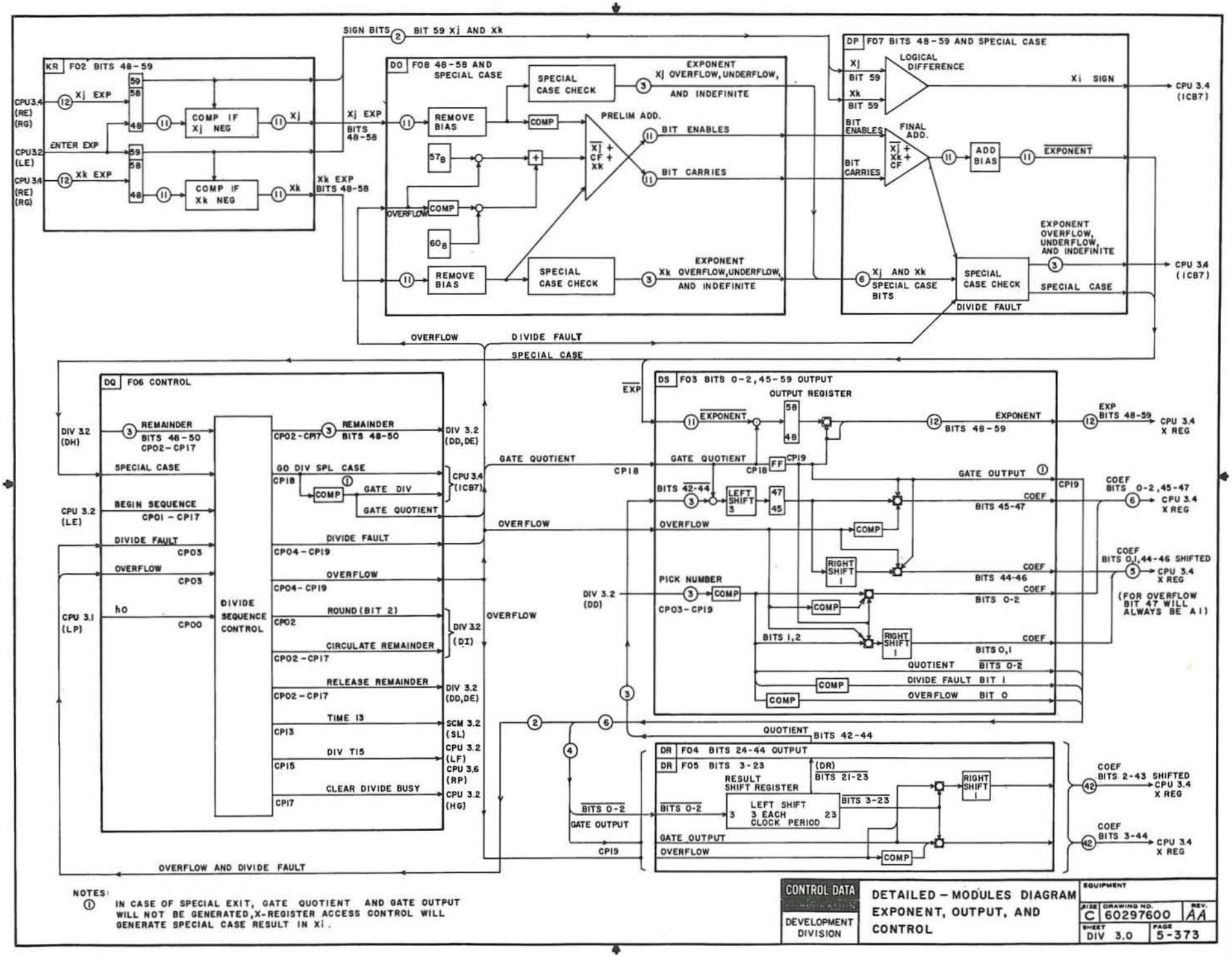
The circulate Remainder signal goes to the four DI modules where it gates the current remainder to the Final Subtraction network. When this signal is a zero, the contents of the Dividend Input register are gated to the Final Subtraction network.

The Release Remainder signal goes to the DD and DE modules. It allows the iteration network to generate a three through a seven. When this signal is a zero, no digit greater than a two can be generated by the iteration network. This signal is a one on the DQ module from CP02 through CP17.

The Time 13 condition originates in the divide sequence control and is used in the SCM access control. This static condition exists during the 14th clock period of execution (The Divide instruction issues during CP00. Thus CP13 is the 14th clock period of instruction execution) for a divide instruction. It is used in the SCM access control to block initiation of a SCM storage reference that would conflict with the delivery of data from the divide unit to the X Register data input path.

The Divide Time 15 condition originates in the divide sequence control and is used in instruction issue control and in the X Register Access Control Unit. This static condition exists during the 16th clock period of execution for a Divide instruction. It is used in the instruction issue control to block issue of an instruction which would conflict with the delivery of data from the divide unit to the X Register data input path. It is used in the X Register access control to initiate the process of register access for the destination X Register.

The Clear Divide Busy condition originates in the divide sequence control and is used to clear the Divide Busy flag. This static condition exists during the 18th clock period of execution for a divide instruction.



NOTES:

① IN CASE OF SPECIAL EXIT, GATE QUOTIENT AND GATE OUTPUT WILL NOT BE GENERATED, X-REGISTER ACCESS CONTROL WILL GENERATE SPECIAL CASE RESULT IN Xi.

CONTROL DATA
DEVELOPMENT DIVISION

DETAILED – MODULES DIAGRAM
EXPONENT, OUTPUT, AND CONTROL

EQUIPMENT

SIZE	DRAWING NO.	REV.
C	60297600	AA
SHEET		PAGE
DIV 3.0		5-373

The divisor (Xk) coefficient input registers are on the four DJ modules. Each DJ module handles 12 bits. Every clock period a 48-bit quantity from the X register arrives at the DJ modules. The sign bit (bit 59) is delivered along with the coefficient. The registers are of the clear enter type which are cleared and new data entered every clock period in which the Enter Xk control signal is a one. When the divide instruction issues on CP00 the Enter Xk is a one. The signal becomes a zero in CP01 and remains a zero until CP18. The data that arrives at the input register in the clock period of instruction issue (CP00) is entered into the register at the end of CP00 and held statically until the end of CP18 when a new quantity is gated into the register. This data is used in executing the divide instruction.

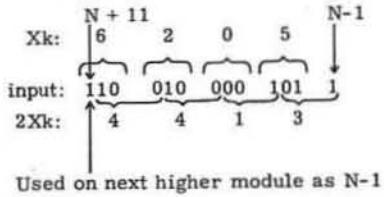
The Divide Unit uses the coefficient magnitude of the operands in executing the divide instructions. Therefore the coefficient must be complemented if it is negative. If the sign bit is a one the operand is negative.

The Xk coefficient magnitude is delivered statically to the multiplication network while the divide process proceeds. The DK, DL, DM, and DN modules form the seven multiples of the divisor coefficient from Xk to 7Xk.

3Xk ADDER

A network on the DK and DN modules creates a 50-bit quantity 3Xk, and from this quantity forms 6Xk. Bits 0-47 of 3Xk are created on the four DK modules, 12 bits to a module. The 12 bits on a DK module are called a section and are referred to as bits N to N + 11. Bits 48 and 49 are created on the DN module.

Each DK module receives 13 bits of Xk from the divisor input registers on the DJ modules. These bits are used by a DK module as both Xk and 2Xk. 2Xk is formed by left shifting Xk one bit position. The 13 Xk bits received are bits N-1 to N + 11. Of these bits N-1 to N + 10 are used as 2Xk bits N to N + 11. Note: N + 11 in one section is N-1 in the next higher section. For example:



The four DK modules form 3Xk by adding bits 0 - 47 of 2Xk to bits 0 - 47 of Xk. A Preliminary Adder on each DK module generates Section Carries and Section Enables.

The DN module receives the four Section Carry bits and three Section Enables from the DK modules and performs carry propagation checks on each section. The carry out of Section 4 (to bit 48) is added to Xk bit 47, which left-shifted one place is considered to be 2Xk bit 48. The sum of this bit and the Section 4 Carry bit produces bits 48 and 49 of 3Xk.

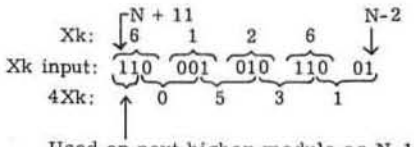
The other three Section Carries are fed back into the Final Add network on the DK modules to produce 3Xk bits 0 - 47.

6Xk NETWORK

6Xk is formed from 3Xk by left shifting one bit position. The multiples are sent to Partial Subtraction and Trial Subtraction networks. Each module in the two subtraction networks handles a three bit group. Therefore each module needs three bits of 3Xk and three bits of 6Xk. The multiplication network sends four 3Xk bits to each module. These bits are labeled bits N-1 to N + 2. Bits N-1 to N + 1 of 3Xk are used by the DA and DH modules as bits N to N + 2 of 6Xk. This is equivalent to left shifting one bit or multiplying by two.

5Xk ADDER

The network that forms 5Xk is on the DL and DN modules. 4Xk is formed by left-shifting Xk two places; 5Xk is formed by adding Xk to this quantity. 5Xk is a 51-bit quantity. The DL modules generates bits 0-47; the DN module generates bits 48-50. Each DL module receives 14 bits of Xk and outputs 12 bits of 5Xk. The 14Xk bits are left shifted two places to form bits N to N + 11 of 4Xk.

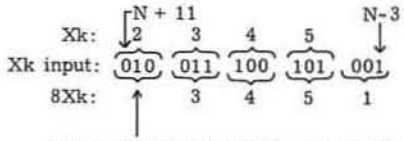


Used on next higher module as N-1 and N-2.

Bits N-2 to N + 9 of Xk are used as bits N to N + 11 of 4Xk. These bits are added to bits N to N + 11 of Xk to form 5Xk. Thus 5Xk is formed by adding 4Xk to Xk. The section carry and enable bits are used in exactly the same manner as in forming 3Xk. The DN module is also used in the same manner as in forming 3Xk.

7Xk SUBTRACTER

The subtractive network that forms 7Xk is on the DM and DN modules. First, 8Xk is formed by left shifting Xk three places. Then 7Xk is formed by subtracting Xk from this quantity. The DM modules generates bits 0-47; the DN module generates bits 48-50. Each DM module receives 15 bits of Xk and outputs 12 bits of 7Xk. The 15Xk bits are left shifted three places to form bits N to N + 11 of 4Xk.

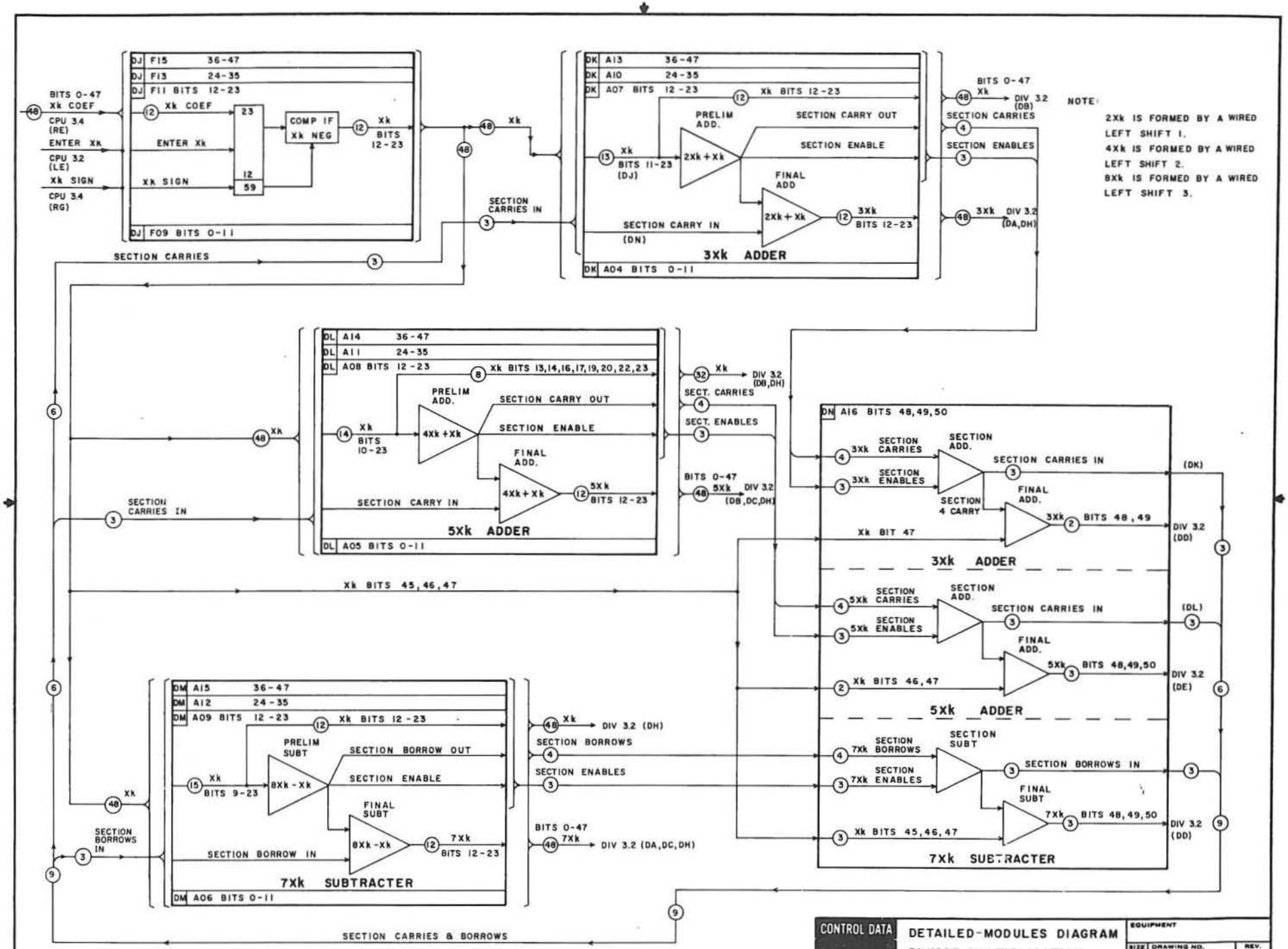


Used on next higher module as N-1 through N-3.

Bits N-3 to N + 8 of Xk are left shifted to become bits N to N + 11 of 8Xk. Bits N to N + 11 of Xk are then subtracted from these bits. Thus 7Xk is formed by subtracting Xk from 8Xk. The section borrows and enables are used in the DN module in the same manner as the section carries and enables were used in forming 3Xk and 5Xk.

Xk, 2Xk, and 4Xk NETWORKS

The networks that form Xk, 2Xk, and 4Xk are on the DK, DL, and DM, modules. These multiples are formed by left shifting the 48 Xk bits. 2Xk is formed by left shifting Xk one bit position and has 49 bits. 4Xk is formed by left shifting Xk two bit positions and has 50 bits. These three multiples are supplied to the Trial Subtraction network and the Partial Subtraction network.


DJ F15 36-47
DJ F13 24-35
DJ F11 BITS 12-23
DJ F09 BITS 0-11
BITS 0-47 Xk COEF
CPU 3.4 (RE)
ENTER Xk
CPU 3.2 (LE)
Xk SIGN
CPU 3.4 (RG)
Xk COEF
ENTER Xk
Xk SIGN
23
12
59
COMP IF Xk NEG
Xk BITS 12-23
SECTION CARRIES IN
SECTION CARRIES
DK A13 36-47
DK A10 24-35
DK A07 BITS 12-23
DK A04 BITS 0-11
Xk BITS 12-23
PRELIM ADD.
SECTION CARRY OUT
SECTION ENABLE
Xk BITS 11-23 (DJ)
2Xk + Xk
FINAL ADD
SECTION CARRY IN (DN)
3Xk BITS 12-23
3Xk ADDER
BITS 0-47 Xk
DIV 3.2 (DB)
SECTION CARRIES
SECTION ENABLES
3Xk DIV 3.2 (DA,DH)
NOTE:
2Xk IS FORMED BY A WIRED LEFT SHIFT 1.
4Xk IS FORMED BY A WIRED LEFT SHIFT 2.
8Xk IS FORMED BY A WIRED LEFT SHIFT 3.
DL A14 36-47
DL A11 24-35
DL A08 BITS 12-23
DL A05 BITS 0-11
Xk BITS 13,14,16,17,19,20,22,23
PRELIM ADD.
SECTION CARRY OUT
SECTION ENABLE
Xk BITS 10-23
4Xk + Xk
FINAL ADD.
SECTION CARRY IN
5Xk BITS 12-23
5Xk ADDER
Xk DIV 3.2 (DB,DH)
SECT. CARRIES
SECT. ENABLES
BITS 0-47 5Xk DIV 3.2 (DB,DC,DH)
DM A15 36-47
DM A12 24-35
DM A09 BITS 12-23
DM A06 BITS 0-11
Xk BITS 12-23
PRELIM SUBT
SECTION BORROW OUT
SECTION ENABLE
Xk BITS 9-23
8Xk - Xk
FINAL SUBT
SECTION BORROW IN
7Xk BITS 12-23
7Xk SUBTRACTER
SECTION BORROWS IN
Xk DIV 3.2 (DH)
SECTION BORROWS
SECTION ENABLES
BITS 0-47 7Xk DIV 3.2 (DA,DC,DH)
DN A16 BITS 48,49,50
3Xk SECTION CARRIES
3Xk SECTION ENABLES
SECTION ADD.
SECTION CARRIES IN
SECTION 4 CARRY
FINAL ADD.
3Xk BITS 48,49
Xk BIT 47
3Xk ADDER
(DK)
DIV 3.2 (DD)
5Xk SECTION CARRIES
5Xk SECTION ENABLES
SECTION ADD.
SECTION CARRIES IN
FINAL ADD.
5Xk BITS 48,49,50
Xk BITS 46,47
5Xk ADDER
(DL)
DIV 3.2 (DE)
7Xk SECTION BORROWS
7Xk SECTION ENABLES
SECTION SUBT
SECTION BORROWS IN
FINAL SUBT
7Xk BITS 48,49,50
Xk BITS 45,46,47
7Xk SUBTRACTER
DIV 3.2 (DD)
Xk BITS 45,46,47
SECTION CARRIES & BORROWS
CONTROL DATA
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM
DIVISOR MULTIPLICATION NETWORK
EQUIPMENT
SIZE C
DRAWING NO. 60297600
REV.
SHEET DIV 3.1
PAGE 5-375

TRIAL SUBTRACTION NETWORK

The Trial Subtraction network determines which of the multiples of the divisor are larger than the current remainder. The Trial Subtraction network also generates a borrow into every three-bit group. The Trial subtraction occurs in two stages.

FIRST STAGE TRIAL SUBTRACTION NETWORK

The First Stage Trial subtraction network generates a borrow and an enable for each three-bit group. The first stage network is on the DA, DB, DC, DD, and DE modules. Each module in this network handles three bits -- one octal digit. Each of the seven multiples of the divisor is subtracted from the remainder. The rank of a subtraction refers to the multiple being subtracted. Thus, the rank 5 subtraction network subtracts 5Xk from the remainder. The DC module handles group 0 (bits 0-2) of all seven ranks. The fifteen DA modules handle groups 1-15 (bits 3-47) of ranks 3, 6, and 7. The DD module handles group 16 (bits 48-50) of ranks 3, 6, and 7. The fifteen DB modules handle groups 1-15 (bits 3-47) of ranks 1, 2, 4, and 5. The DE module handles group 16 (bits 48-50) of ranks 1, 2, 4, and 5.

The data for the First Stage Subtraction comes from two sources. The remainder is held within each module from the Final Subtraction on the previous iteration.

Each module in the First Stage Trial Subtraction network handles a three-bit group -- one octal digit. The remainder digit is compared with each of the multiples on a module. If a remainder digit is the same as a multiple digit, the enable for that group and that multiple digit is larger than that remainder digit. The DC module does not generate any enables since no borrow can be propagated through bits 0-2.

The control signals into the DD and DE modules can force the rank 1-7 group 16 borrow out bits to be ones. If these borrow bits are ones, the EAB bits for the corresponding ranks are ones, and rank 0 is selected for the final subtraction. The Release Remainder signal from the DQ module into the DD and DE modules forces the rank 3-7 group 16 borrow out bits to ones. The Release Rank 1, 2 Borrows signal into the DE module from the LE module forces the rank 1 and 2 borrow out bits to ones. These signals are used in CP01 and CP02.

In CP01 both signals are zeros; the rank 1-7 group 16 borrow out bits are all ones the rank 1-7 EAB bits are all ones; the Final Subtraction network selects rank 0 for the final subtraction; the dividend is selected by the DI modules as the rank 0 bit enables; and the dividend is gated into the Remainder Register.

In CP02, the DD and DE modules receive the Release Remainder signal from the DQ module. This signal was set to a zero by the DQ module in CP01. The DD and DE modules complement this signal to a one and use it to force the rank 3-7 group 16 borrow out bits to ones. This causes the rank 3-7 EAB bits to be ones and the Final Subtraction network selects one of the ranks 0, 1, or 2 for the Final Subtraction. Thus, if the dividend exceeds the divisor by a factor of two or more the DD module generates a two as the first quotient digit.

SECOND STAGE TRIAL SUBTRACTION NETWORK

The outputs of the First Stage Trial Subtraction network go to the Second Stage Trial Subtraction network on the DG and DF modules. The Second Stage Trial Subtraction network determines which multiples of divisor are larger than the remainder and generates borrows into all groups for every rank. Each of the seven DF modules handles a different one of the seven ranks. The same is true of the seven DG modules. One DF module and one DG module together handle one rank.

The DF and DG modules receive identical inputs. Each module in the second stage network receives 17 borrows, one from each of the 17 groups, and 16 enables, one from each of 16 groups. All the inputs to one module pertain to the same rank.

The second stage network determines which multiples are larger than the remainder. If remainder is smaller than the multiple, that rank subtraction will generate an end around borrow (EAB). Each DF and each DG module generates an EAB bit for its rank. If the EAB bit for a particular rank is a one, the remainder is smaller than the multiple. If this EAB bit is a zero, the remainder is greater than or equal to the multiple. These bits are sensed in the Final Subtraction network to determine which multiple to use for the Final Subtraction. The DF bit goes to every DA and DD module. The DG bit goes to every DB and DE module. The EAB bit generated by the DE module is a duplicate of the EAB bit generated by the DG module. This duplication is simply an additional means of fanning out the EAB bit to all the destination modules.

The Second Stage network generates a borrow into groups 3-16 for each rank. Each DF module generates borrows into groups 3, 5, 7, 9, 11, 13, and 15 for its rank. Each DG module generates borrows into groups 4, 6, 8, 10, 12, 14, and 16 for its rank. The DF and DG modules generate the group borrow inputs for each group in the normal fashion. However, in transmitting the group borrow inputs to the destination DA, DB, DD, and DE modules the group borrow inputs are left shifted one group to align them properly with the inclusive bit enables from the DH modules. Thus, instead of generating a group borrow into group 8, the following conditions will generate a borrow into group 9: group 7 generated a borrow out; group 6 generated a borrow out and group 7 generated an enable; any of groups 0-5 generated a borrow and all the higher groups (up to and including group 7) generated an enable.

PARTIAL SUBTRACTION NETWORK

The Partial Subtraction network provides the inclusive bit enables used in the Final Subtraction. The Partial Subtraction network is on the 16 DH modules. Bits 0-47 are divided into 16 three-bit groups (ie. into 16 octal digits) with one digit per module.

The Partial Subtraction network receives the complemented Remainder from the Remainder Register and seven multiples of the remainder from the Multiplication network. The subtraction network combines the $\overline{\text{Remainder}}$ bits and the multiple bits to generate inclusive bit enables. Each DH module adds the $\overline{\text{Remainder}}$ digit to each of the seven multiples.

The outputs of the Partial Subtraction network go to the Final Subtraction network. All the outputs from the Partial Subtraction network are left-shifted one octal digit (i.e. three binary bits). The $\overline{\text{Remainder}}$ (rank 0 inclusive bit enables) is recomplemented to generate the true remainder bits. Remainder bits 45-57 are sent to the DQ module and bits 0-44 to four DI modules. Because of the 3-bit left-shift these bits are labeled bits 48-50 at the DQ module and bits 3-47 at the DI modules. The results of the computation -- seven octal digits on each module -- are sent to the Final Subtraction network on the DA and DB modules. The seven octal digits from DH-E16 are sent to the DD and DE modules. Because of the left-shift these are bits 3-50 enables.

The Remainder digits (rank 0 inclusive bit enables) go through an intermediate network on the DI and DQ modules before they are transmitted to the final subtraction network. The DQ module gates bits 48-50 to the Final Subtraction network in the DD and DE modules in clock periods CP02 through CP17 only. The Circulate Remainder signal in the DI modules chooses either the remainder bits 3-47 or the quantity in the Dividend Register.

In CP01 the dividend from the divide sequence is in the dividend register. In CP01, therefore, the complemented dividend is gated to the Final Subtraction network. During CP02 thru CP17 the complemented remainder is gated to the Final Subtraction network. In CP02-CP17 bits 0-2 are always zeros with one exception. Bit 2 will be a one in CP02 if the instruction is a round floating divide. All output bits (bits 0-47 from the DI modules and bits 48-50 from the DQ module) are complemented to become rank 0 inclusive bit enables before transmission to the Final Subtraction network.

During a round floating divide instruction, a round bit is added to the dividend which has the effect of increasing the dividend by one half count. The effect this has on the quotient will vary depending on the value of the divisor and on the truncation point in the quotient. If the dividend is smaller than the divisor the quotient will be truncated one bit position lower than if the dividend is equal to, or larger than, the divisor. These effects cause the rounding to vary in the quotient from a value of 1/4 of the least significant bit in the result to almost one. The average rounding bias over the entire range of coefficient values is zero.

When a divide instruction is executed, the h0 (round) bit is held in the DQ (control) module. If the instruction is a round floating divide instruction this bit will be a one. If the instruction is a floating divide instruction this bit will be a zero. The DQ module holds this round bit until CP02, when it is transmitted to the DI-F10 module. This bit then becomes bit 2 of the rank 0 inclusive bit enables. Since bit 2 of the rank 0 bit enables is normally a zero, the round bit has an effect only on round instructions (when the round bit is a one). The DC module enters the rank 0 bit 0-2 enables into the Remainder register every clock period.

FINAL SUBTRACTION NETWORK

The Final Subtraction network picks one rank, completes that rank subtraction, and gates the result into the remainder register. An octal digit (Pick Number) corresponding to the chosen rank is gated into the quotient shift register. The Remainder is then available to the First Stage Trial Subtraction network and the Partial Subtraction network.

The Final Subtraction network is on the DA, DB, DD, and DE modules. The DA and DB modules have identical final subtraction networks, as do the DD and DE modules. The DA modules output $\overline{\text{Remainder}}$ bits to the Partial Subtraction network. The DD module generates the Pick Number. Each module in this network handles a three-bit group. The 15 DA and the 15 DB modules handle groups 1-15, bits 3-47. The DD and DE modules handle group 16, bits 48-50. Group 0, bits 0-2 is handled in the DC module and will be discussed later.

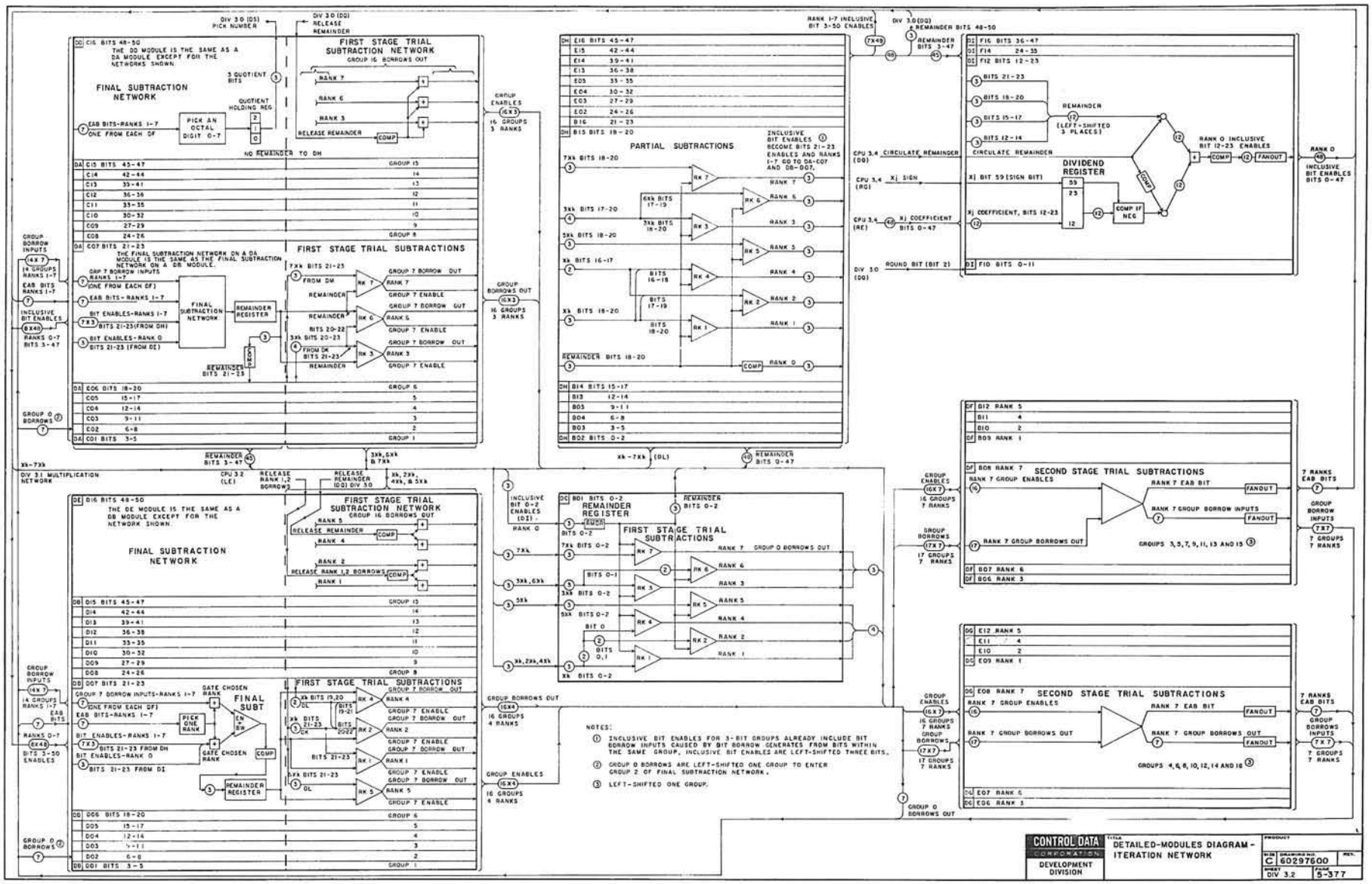
The inputs to the Final Subtraction network come from the Second Stage Trial Subtraction network and the Partial Subtraction network. Each module in the Final Subtraction network receives seven EAB bits, one for each rank. Each DA or DD module receives one EAB from each of the seven DF modules. Each DB or DE module receives one EAB from each of the seven DG modules. Each module in the Final network receives a group borrow input for each of ranks 1-7 from the Second Stage Trial Subtraction network. DA-C02 and DB-D02 receive group 0 borrows (shifted left one group) from the DC module. All other modules in this network receive inputs from a DF or a DG module, depending of the group handled. Each module in the network receives three enable bits for each of the eight ranks. The ranks 1-7 enables come from the DH modules, the rank 0 enables come from the DI modules. The group 16 (bits 48-50) rank 0 enables come from the DQ module.

The data is combined to generate three remainder bits for each module. The EAB bits are sensed, and the largest rank that did not produce EAB is used for the final subtraction. The borrow bit for that rank is added to the octal digit and the sum is complemented. The result is entered into the Remainder Register.

A network on DD module senses the EAB bits and generates a Pick Number. The digit generated is the same as the rank chosen for the final subtraction. This digit is entered into a register and sent from there to the coefficient Shift Register on the DS module.

The DC module holds group 0, bits 0-2 of the remainder. In CP01 bits 0-2 of the dividend are entered into the Remainder register. In CP02-CP17, zero bits are entered into bits 0-2. During a round floating divide instruction, a one is entered in bit 2 in CP02. This bit increases the value of the dividend by one-half a count.

Bits 0-47 of the remainder are sent to the Partial Subtraction network. These bits are transmitted from the DC and DA modules to the DH modules.

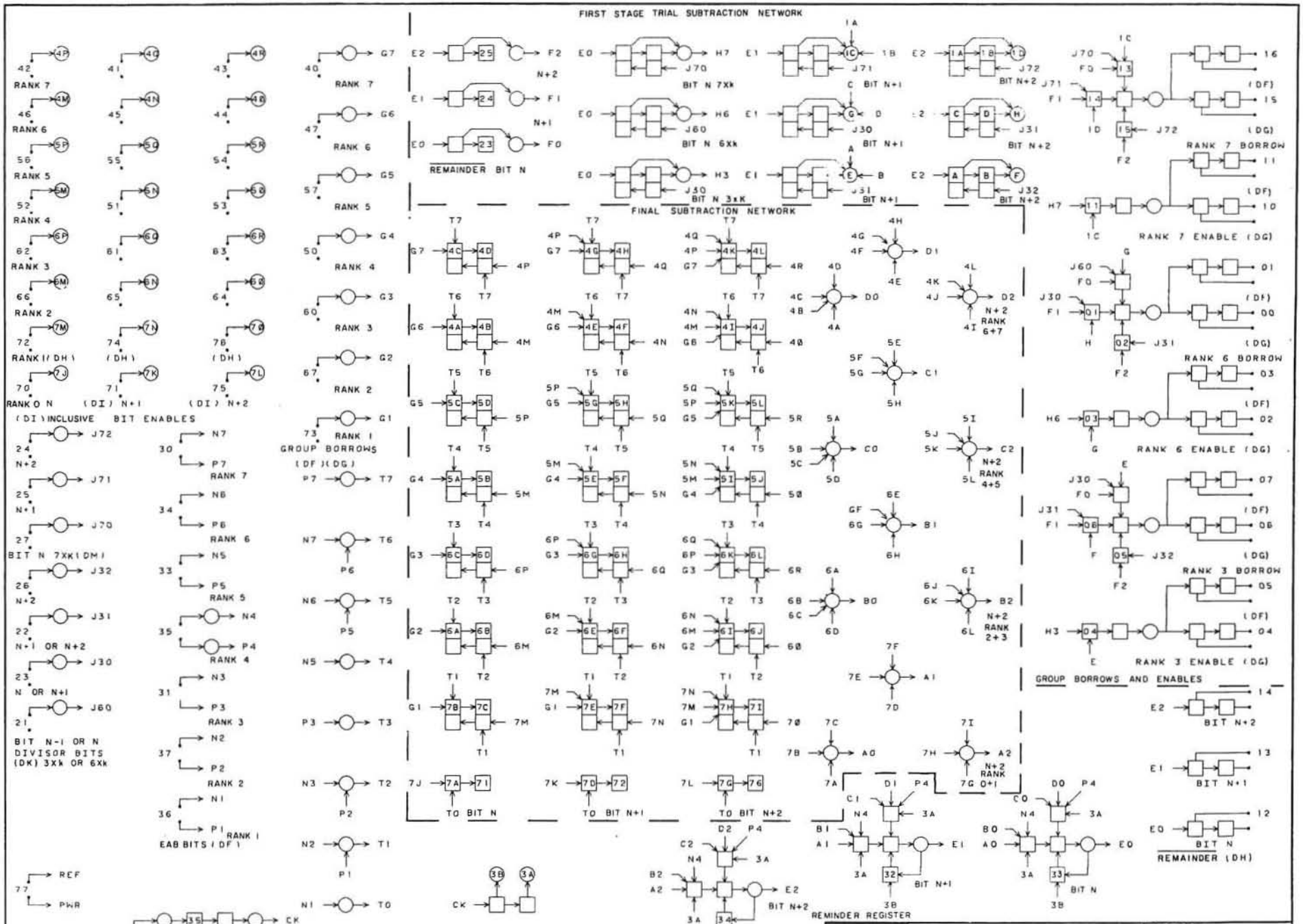

FIRST STAGE TRIAL SUBTRACTION NETWORK
FINAL SUBTRACTION NETWORK
FIRST STAGE TRIAL SUBTRACTIONS
PARTIAL SUBTRACTIONS
DIVIDEND REGISTER
REMAINDER REGISTER
SECOND STAGE TRIAL SUBTRACTIONS
NOTES:
① INCLUSIVE BIT ENABLES FOR 3-BIT GROUPS ALREADY INCLUDE BIT BORROW INPUTS CAUSED BY BIT BORROW GENERATES FROM BITS WITHIN THE SAME GROUP. INCLUSIVE BIT ENABLES ARE LEFT-SHIFTED THREE BITS.
② GROUP 0 BORROWS ARE LEFT-SHIFTED ONE GROUP TO ENTER GROUP 2 OF FINAL SUBTRACTION NETWORK.
③ LEFT-SHIFTED ONE GROUP.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
DETAILED-MODULES DIAGRAM - ITERATION NETWORK
C 60297600
DIV 3.2
5-377

DA MODULE

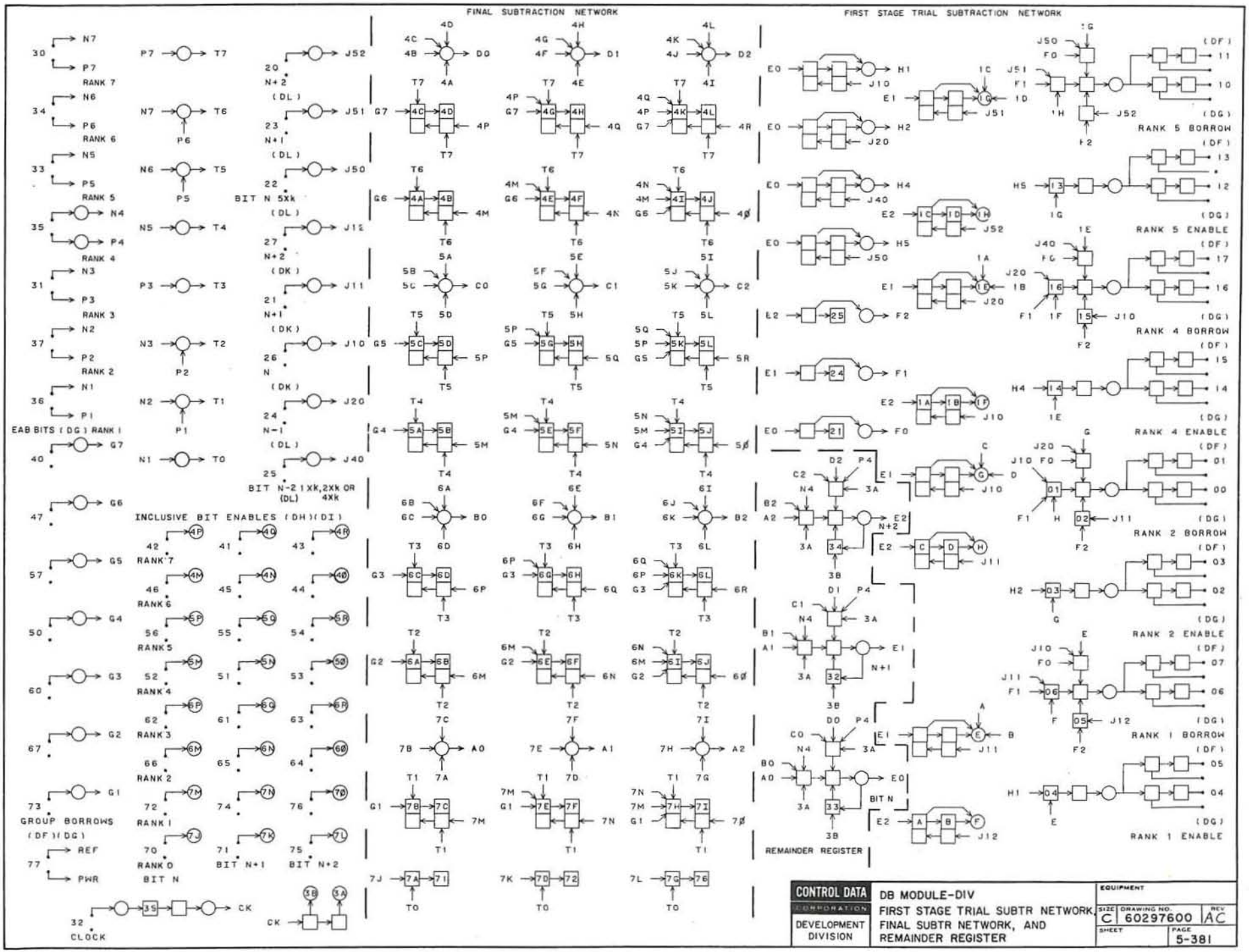
The 15 DA modules function in the First Stage Trial Subtraction and the Final Subtraction networks. These modules also hold 45 bits of the Remainder register, three bits on each module.

In the First Stage Trial Subtraction network 3Xk, 6Xk, and 7Xk are subtracted from the current Remainder. Bits 0, 1, and 2 of the remainder are contained in the E0, E1, and E2 flip-flops in the lower right hand corner of the drawing. The J60, J30, J31, and J32 input terms on the left are bits N-1 to N + 2 of 3Xk. Of these, J60, J30, and J31 are also used as bits N to N + 2 of 6Xk. The J70, J71, and J72 input terms are bits N to N + 2 of 7Xk. These 3Xk, 6Xk, and 7Xk terms are subtracted from the remainder terms in the network on the upper right of the drawing. The output is the group borrow out and group enable bits on the right of the drawing.

In the Final Subtraction network the bit enables from one of the eight ranks are added to the group borrows from the same rank, the result is complemented and entered into the Remainder Register. The seven EAB bits, which are the N1 to N7 terms just to the right of the J60 to J72 terms, are sensed to choose one or two ranks for the final subtraction. The T0 to T7 terms are the first part of the selection process. One of the four terms T0, T1, T2, or T3 is a one, and one of the terms T4, T5, T6, and T7 is also a one. The network in the middle of the page performs the final subtraction of the two ranks whose T terms are ones. The results of the two final subtractions are complemented. If the N4 term is a one the result from one of ranks 4-7 is gated into the remainder register. If the N4 term is a zero, the P4 term is a one and the result from one of ranks 0-3 is gated into the Remainder Register. The terms used in the final subtractions are the inclusive bit enable and the group borrows in the upper left corner of the page. The three Remainder Bits are complemented and sent to a DH module.



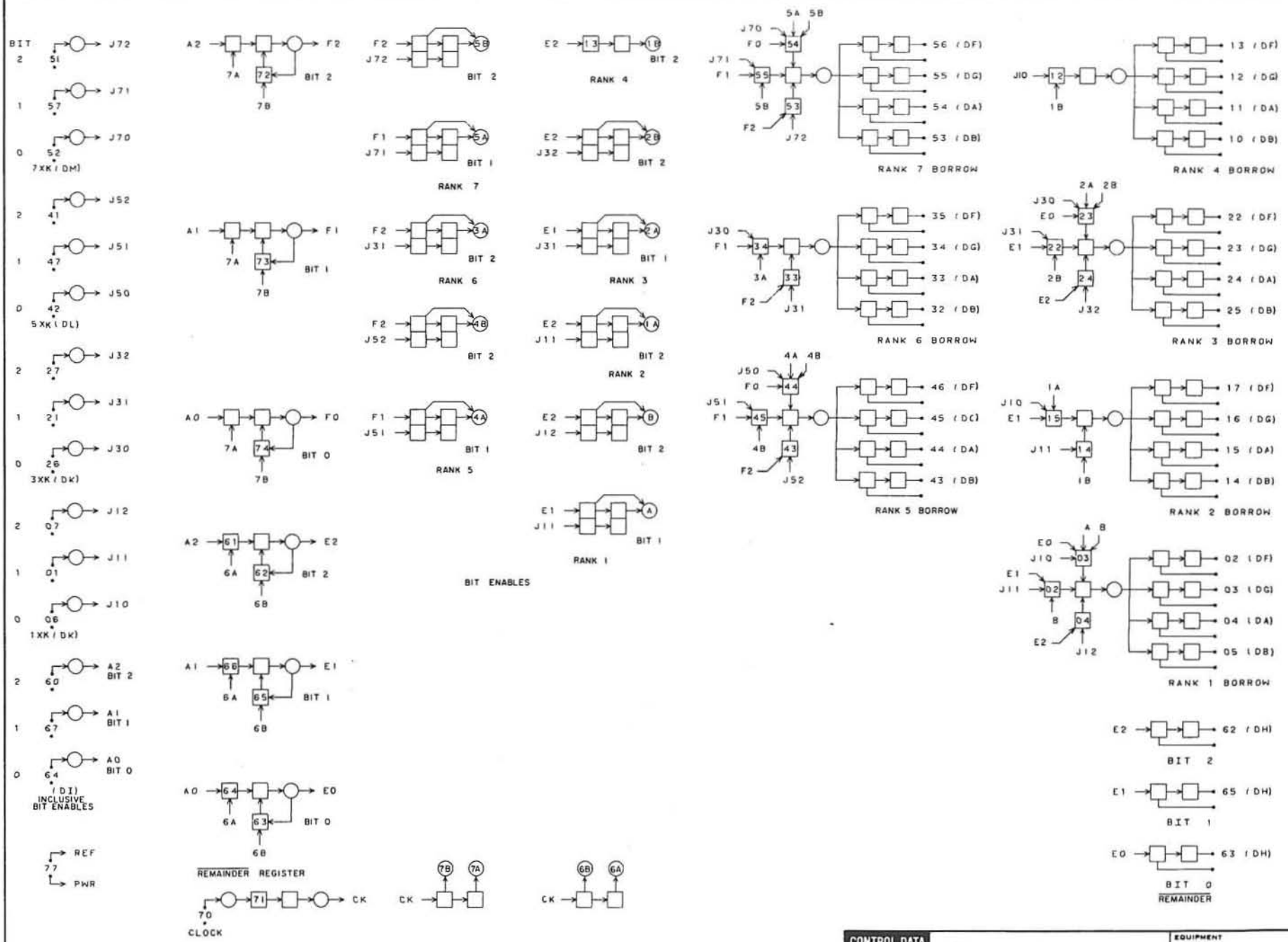
CONTROL DATA INFORMATION DEVELOPMENT DIVISION	DA MODULE-DIV-FIRST STAGE TRIAL SUBTR NETWORK, FINAL SUBTR NETWORK AND REMAINDER REGISTER	EQUIPMENT SIZE C DRAWING NO. 60297600 REV. SHEET PAGE 5-379	


FINAL SUBTRACTION NETWORK
FIRST STAGE TRIAL SUBTRACTION NETWORK
RANK 7
RANK 6
RANK 5
RANK 4
RANK 3
RANK 2
RANK 1
RANK 0
EAB BITS (DG) RANK 1
INCLUSIVE BIT ENABLES (DH)(DI)
GROUP BORROWS (DF)(DG)
REF
PWR
CLOCK
BIT N
BIT N+1
BIT N+2
BIT N 5Xk
BIT N-2 1Xk,2Xk OR 4Xk (DL)
N
N+1
N+2
REMAINDER REGISTER
RANK 5 BORROW
RANK 5 ENABLE
RANK 4 BORROW
RANK 4 ENABLE
RANK 2 BORROW
RANK 2 ENABLE
RANK 1 BORROW
RANK 1 ENABLE
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
DB MODULE-DIV
FIRST STAGE TRIAL SUBTR NETWORK, FINAL SUBTR NETWORK, AND REMAINDER REGISTER
EQUIPMENT
SIZE C
DRAWING NO. 60297600
REV AC
SHEET
PAGE 5-381

The DC module functions in the Trial Subtraction network. The seven divisor multiples are subtracted from the remainder. The A0, A1, and A2 terms are inclusive bit 0-2 enables. These terms are entered into the Remainder Register, F0, F1, and F2 and E0, E1, and E2 as $\overline{\text{Remainder}}$. Since the bit enables are all complements of the remainder, the E and F terms are complements of the remainder.

The JXX terms represent the seven multiples. The J1X terms are Xk; the J3X terms are 3Xk; the J5X terms are 5Xk; the J7X terms are 7Xk. 2Xk, 4Xk, and 6Xk are formed by shifting the Xk and 3Xk terms. J10 and J11 are used as bits 1 and 2 of 2Xk. Bit 0 of 2Xk is taken as a zero. J10 is used as bit 2 of 4Xk. Bits 0 and 1 of 4Xk are taken as zeros. J30 and J31 are used as bits 1 and 2 of 6Xk. Bit 0 is taken to be a zero.

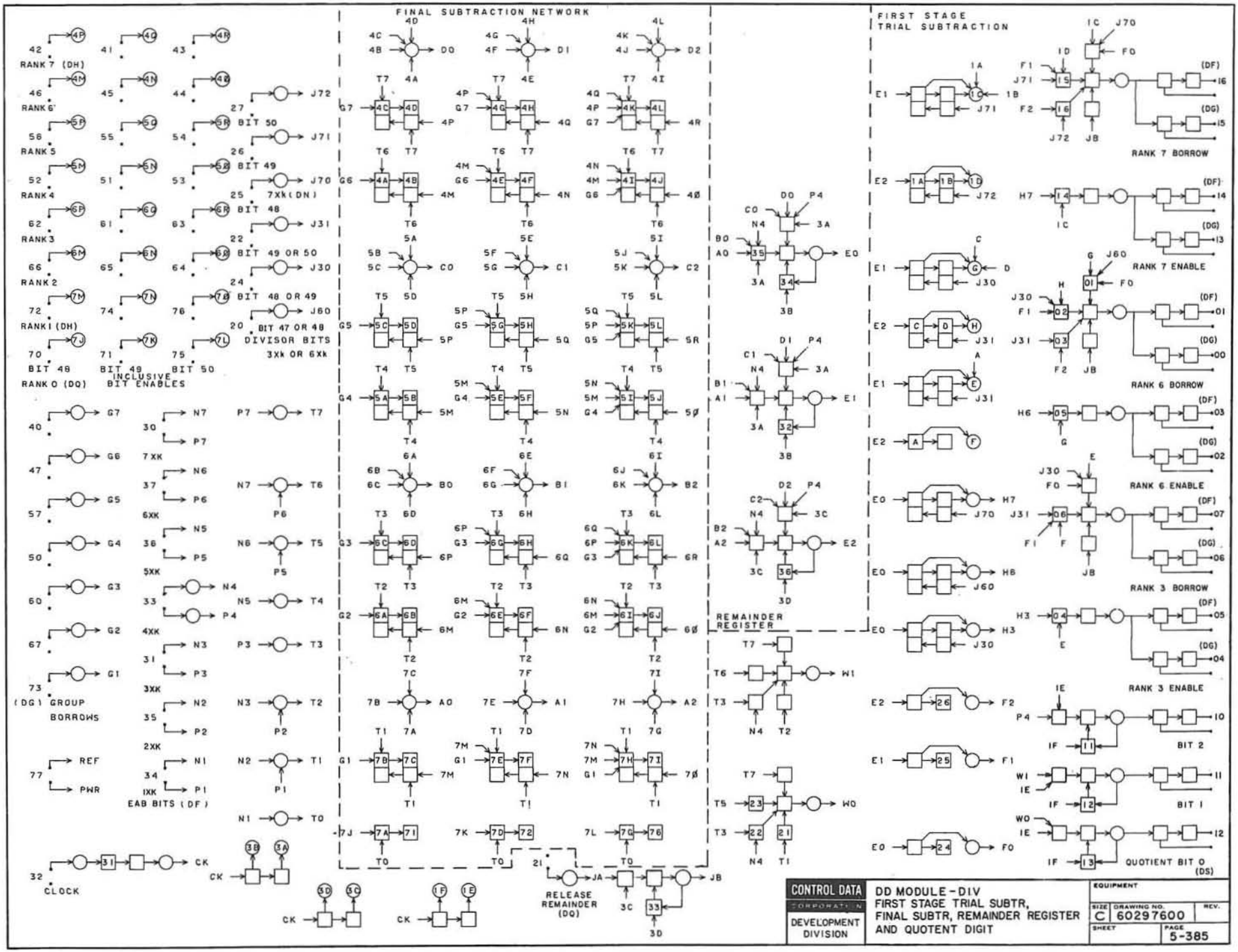
The XA and XB terms are bit enables. The $\overline{\text{Remainder}}$, multiples, and enables are combined to generate group 0 borrows for ranks 1-7. These borrows are sent to the Second Stage Trial Subtraction network and the Final Subtraction network.



CONTROL DATA CORPORATION	DC MODULE - DIV TRIAL SUBTR NETWORK, AND REMAINDER REGISTER	EQUIPMENT	
DEVELOPMENT DIVISION		SIZE C	DRAWING NO. 60297600
		SHEET	PAGE 5-383

DD MODULE

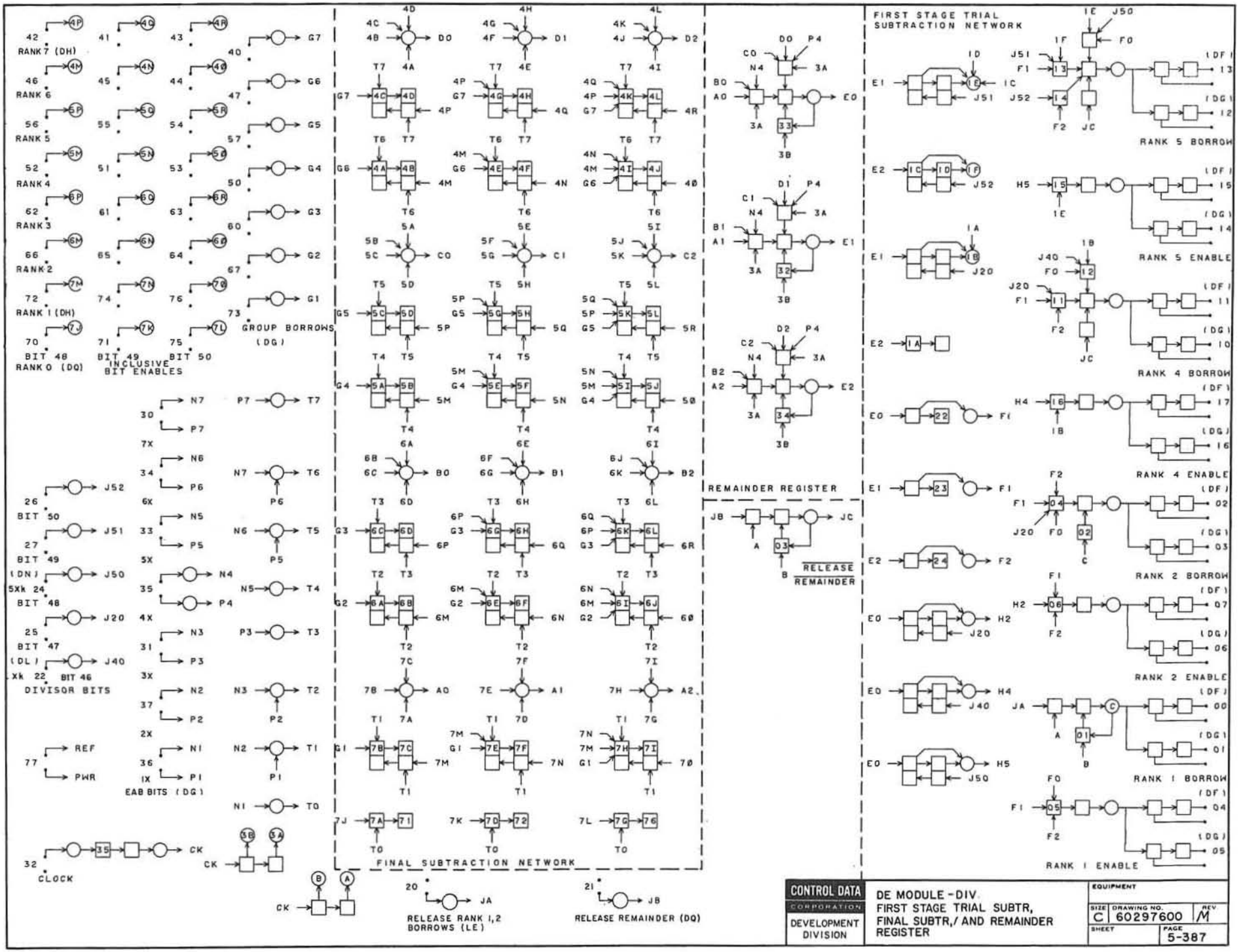
The DD module is like a DA module except for three differences. The first difference is that no remainder bits are sent to the Partial Subtraction network. The second difference is that the Release Remainder signal from the DQ module forces the group 16 borrows for ranks 3, 6, and 7 to ones in CP01 and CP02. These borrows force the EAB bits for the corresponding ranks to be ones also. These terms are forced to ones in CP01 to choose rank 0 for the final subtraction and thereby gate the dividend into the remainder register. These terms are forced to ones in CP02 to choose one of ranks 0, 1, or 2 for the final subtraction and thereby insure that if a divide fault condition exists it will be detected. The third difference is that the DD module generates a quotient octal digit every clock period. The W0 and W1 terms represent bits 0 and 1 of the quotient digit. P4 represents bit 2 of the quotient digit.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	DD MODULE - DIV FIRST STAGE TRIAL SUBTR, FINAL SUBTR, REMAINDER REGISTER AND QUOTENT DIGIT	EQUIPMENT	
		SIZE C	DRAWING NO. 60297600
		SHEET	PAGE 5-385

DE MODULE

The DE module is like a DB module except for two differences. The first of these differences is the Release Rank 1, 2 Borrows signal, JA, from the LE module. This signal forces the rank 1 and rank 2 group 16 borrows out to be ones in CP01. These borrows in turn force the rank 1 and rank 2 EAB bits to be ones in CP01. The EAB bits choose rank 0 for the final subtraction and thereby gate the dividend into the Remainder Register. The second difference is the Release Remainder signal, JB, from the DQ module. This signal forces the rank 4 and 5 group 16 borrows out to be ones in CP01 and CP02. These borrows in turn force the rank 4 and 5 EAB bits to be ones in CP01 and CP02. The EAB bits choose rank 0 for the final subtraction in CP01 and thereby gate the dividend into the Remainder Register. In CP02 the EAB bits choose one of ranks 0, 1, or 2 for the final subtraction and thereby ensure that if a divide fault condition exists it will be detected.


RANK 7 (DH)
RANK 6
RANK 5
RANK 4
RANK 3
RANK 2
RANK 1 (DH)
BIT 48 RANK 0 (DQ)
BIT 49 INCLUSIVE BIT ENABLES
BIT 50
GROUP BORROWS (DG)
DIVISOR BITS
EAB BITS (DG)
CLOCK
FINAL SUBTRACTION NETWORK
REMAINDER REGISTER
RELEASE REMAINDER
RELEASE RANK 1,2 BORROWS (LE)
RELEASE REMAINDER (DQ)
FIRST STAGE TRIAL SUBTRACTION NETWORK
RANK 5 BORROW
RANK 5 ENABLE
RANK 4 BORROW
RANK 4 ENABLE
RANK 2 BORROW
RANK 2 ENABLE
RANK 1 BORROW
RANK 1 ENABLE
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
DE MODULE - DIV
FIRST STAGE TRIAL SUBTR, FINAL SUBTR, / AND REMAINDER REGISTER
EQUIPMENT
SIZE C
DRAWING NO. 60297600
REV. M
SHEET
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